# LM380

## *AN-69 LM380 Power Audio Amplifier*

Literature Number: SNAA086

# LM380 Power Audio Amplifier

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LM380 Power Audio Amplifier

## INTRODUCTION

The LM380 is a power audio amplifier intended for consumer applications. It features an internally fixed gain of 50 (34 dB) and an output which automatically centers itself at one-half of the supply voltage. A unique input stage allows inputs to be ground referenced or AC coupled as required. The output stage of the LM380 is protected with both short circuit current limiting and thermal shutdown circuitry. All of these internally provided features result in a minimum external parts count integrated circuit for audio applications.

This paper describes the circuit operation of the LM380, its power handling capability, methods of volume and tone control, distortion, and various application circuits such as a bridge amplifier, a power supply splitter, and a high input impedance audio amplifier.

## CIRCUIT DESCRIPTION

*Figure 1* shows a simplified circuit schematic of the LM380. The input stage is a PNP emitter-follower driving a PNP differential pair with a slave current-source load. The PNP input is chosen to reference the input to ground, thus enabling the input transducer to be directly coupled.

The output is biased to half the supply voltage by resistor ratio $R_1/R_2$. Negative DC feedback, through resistor $R_2$, balances the differential stage with the output at half supply, since $R_1 = 2 R_2$ (*Figure 1*).

The second stage is a common emitter voltage gain amplifier with a current-source load. Internal compensation is provided by the pole-splitting capacitor C′. Pole-splitting compensation is used to preserve wide power bandwidth (100 kHz at 2W, 8Ω). The output is a quasi-complementary pair emitter-follower.

The amplifier gain is internally fixed to 34 dB or 50. This is accomplished by the internal feedback network $R_2$–$R_3$. The gain is twice that of the ratio $R_2/R_3$ due to the slave current-source which provides the full differential gain of the input stage.

**TABLE I. Electrical Characteristics (Note 1)**

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Output (rms) | 8Ω loads, 3% T.H.D. (Notes 3,4) | 2.5 | | | Wrms |
| Gain | | 40 | 50 | 60 | V/V |
| Output Voltage Swing | 8Ω load | | 14 | | $V_{p\text{-}p}$ |
| Input Resistance | | | 150k | | Ω |
| Total Harmonic Distortion | $P_o = 1W$, (Notes 4 & 5) | | 0.2 | | % |
| Power Supply Rejection | $C_{bypass} = 5\ \mu F$, † = 120 Hz (Note 2) | | 38 | | dB |
| Supply Voltage Range | | 8 | | 22 | V |
| Bandwidth | $P_o = 2W$, $R_L = 8\Omega$ | | 100k | | Hz |
| Quiescent Output Voltage | | 8 | 9 | 10 | V |
| Quiescent Supply Current | | | 7 | 25 | mA |
| Short Circuit Current | | | 1.3 | | A |

**Note 1:** $V_S = 18V$; $T_A = 25°C$ unless otherwise specified.

**Note 2:** Rejection ratio referred to output.

**Note 3:** With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16″ epoxy glass board with 2 ounce copper foil with a minimum surface of six square inches.

**Note 4:** If oscillation exists under some load conditions, add a 2.7Ω resistor and 0.1 μF series network from Pin 8 to ground.

**Note 5:** $C_{bypass} = 0.47\ \mu F$ on Pin 1.

**Note 6:** Pins 3, 4, 5, 10, 11, 12 at 50°C derates 25°C/W above 50°C case.

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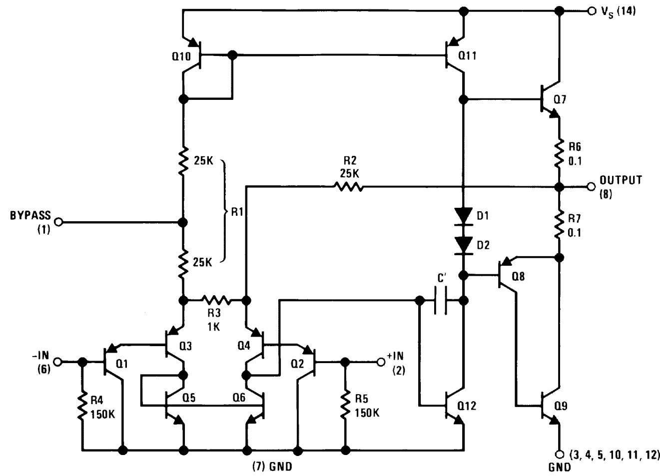


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**FIGURE 1**

**GENERAL OPERATING CHARACTERISTICS**

The output current of the LM380 is rated at 1.3A peak. The 14 pin dual-in-line package is rated at 35°C/W when soldered into a printed circuit board with 6 square inches of 2 ounce copper foil (*Figure 2*). Since the device junction temperature is limited to 150°C via the thermal shutdown circuitry, the package will support 3 watts dissipation at 50°C ambient or 3.7 watts at 25°C ambient.

*Figure 2* shows the maximum package dissipation versus ambient temperature for various amounts of heat sinking.

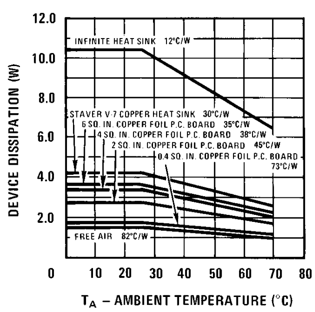


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**FIGURE 2. Device Dissipation vs Ambient Temperature**

*Figures 3a, b,* and *c* show device dissipation versus output power for various supply voltages and loads.

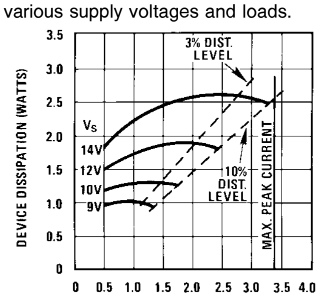


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**FIGURE 3a. Device Dissipation vs Output Power — 4Ω Load**

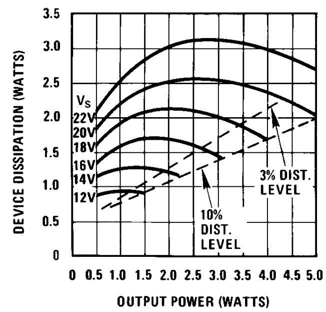


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**FIGURE 3b. Device Dissipation vs Output Power — 8Ω Load**

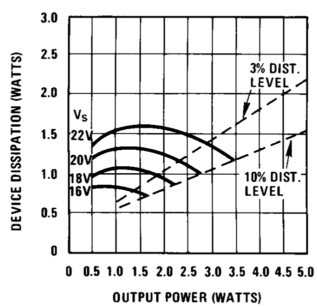


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**FIGURE 3c. Device Dissipation vs Output Power — 16Ω Load**

The maximum device dissipation is obtained from *Figure 2* for the heat sink and ambient temperature conditions under which the device will be operating. With this maximum allowed dissipation, *Figures 3a, b* and *c* show the maximum power supply allowed (to stay within dissipation limits) and the output power delivered into 4, 8 or 16Ω loads. The three percent total-harmonic distortion line is approximately the on-set of clipping.

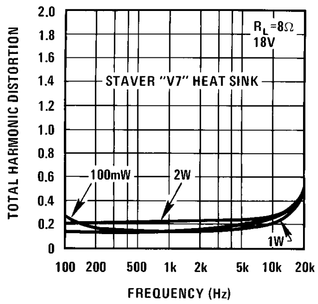


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**FIGURE 4. Total Harmonic Distortion vs Frequency**

*Figure 4* shows total harmonic distortion versus frequency for various output levels, while *Figure 5* shows the power bandwidth of the LM380.

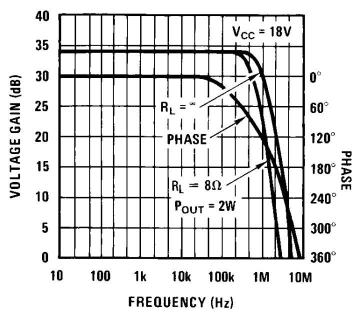


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**FIGURE 5. Output Voltage Gain vs Frequency**

Power supply decoupling is achieved through the AC divider formed by $R_1$ (Figure 1) and an external bypass capacitor. Resistor $R_1$ is split into two 25 kΩ halves providing a high source impedance for the integrator. *Figure 6* shows supply decoupling versus frequency for various bypass capacitors.

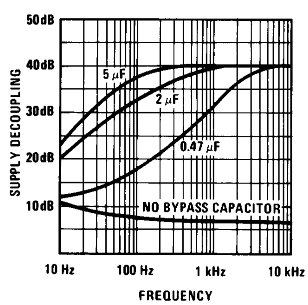


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**FIGURE 6. Supply Decoupling vs Frequency**

## BIASING

The simplified schematic of *Figure 1* shows that the LM380 is internally biased with the 150 kΩ resistance to ground. This enables input transducers which are referenced to ground to be direct-coupled to either the inverting or non-inverting inputs of the amplifier. The unused input may be either: 1) left floating, 2) returned to ground through a resistor or capacitor or 3) shorted to ground. In most applications where the non-inverting input is used, the inverting input is left floating. When the inverting input is used and the non-inverting input is left floating, the amplifier may be found to be sensitive to board layout since stray coupling to the floating input is positive feedback. This can be avoided by employing one of three alternatives: 1) AC grounding the unused input with a small capacitor. This is preferred when using high source impedance transducer. 2) Returning the unused input to ground through a resistor. This is preferred when using moderate to low DC source impedance transducers and when output offset from half supply voltage is critical. The resistor is made equal to the resistance of the input transducer, thus maintaining balance in the input differential amplifier and minimizing output offset. 3) Shorting the unused input to ground. This is used with low DC source impedance transducers or when output offset voltage is non-critical.

## OSCILLATION

The normal power supply decoupling precautions should be taken when installing the LM380. If $V_S$ is more than 2″ to 3″ from the power supply filter capacitor it should be decoupled with a 0.1 µF disc ceramic capacitor at the $V_S$ terminal of the IC.

The $R_C$ and $C_C$ shown as dotted line components on *Figure 7* and throughout this paper suppresses a 5 to 10 MHz

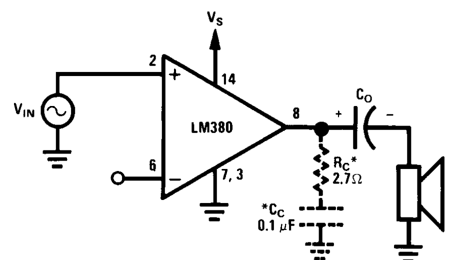


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**FIGURE 7. Minimum Component Configuration**

small amplitude oscillation which can occur during the negative swing into a load which draws high current. The oscillation is of course at too high of a frequency to pass through a speaker, but it should be guarded against when operating in an RF sensitive environment.

## APPLICATIONS

With the internal biasing and compensation of the LM380, the simplest and most basic circuit configuration requires only an output coupling capacitor as seen in *Figure 7*.

An application of this basic configuration is the phonograph amplifier where the addition of volume and tone controls is required. *Figure 8* shows the LM380 with a voltage divider volume control and high frequency roll-off tone control.

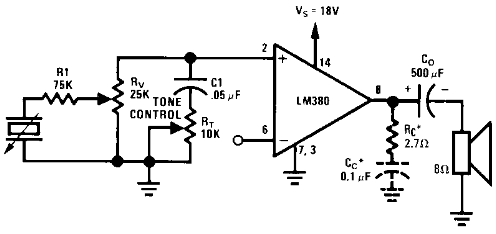


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**FIGURE 8. Phono Amp**

When maximum input impedance is required or the signal attenuation of the voltage divider volume control is undesirable, a ''common mode'' volume control may be used as seen in *Figure 9*.

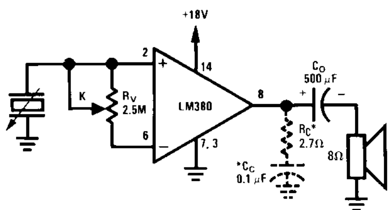


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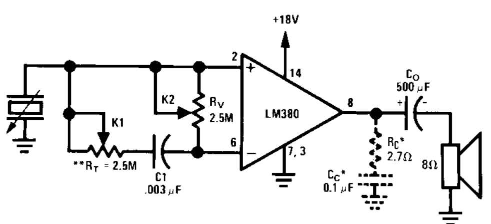
**FIGURE 9. ''Common Mode'' Volume Control**

With this volume control the source loading impedance is only the input impedance of the amplifier when in the full-volume position. This reduces to one-half the amplifier input impedance at the zero volume position. Equation 1 describes the output voltage as a function of the potentiometer setting.

$$V_{OUT} = 50\,V_{IN}\left(1 - \frac{150 \times 10^3}{k_1R_V + 150 \times 10^3}\right)_{0\,\le k_1\,\le\,1} \quad (1)$$

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**Audio Tape Potentiometer (10% of $R_T$ at 50% Rotation)

**FIGURE 10. ''Common Mode'' Volume and Tone Control**

This ''common mode'' volume control can be combined with a ''common mode'' tone control as seen in *Figure 10*.

This circuit has a distinct advantage over the circuit of *Figure 7* when transducers of high source impedance are used, in that, the full input impedance of the amplifier is realized. It also has an advantage with transducers of low source impedance since the signal attenuation of the input voltage divider is eliminated. The transfer function of the circuit of *Figure 10* is given by:

$$\frac{V_{OUT}}{V_{IN}} = 50\left(1 - \frac{150k}{150k + \dfrac{k_1R_Tk_2R_V + \dfrac{k_2R_V}{j2\pi fc_1}}{k_1R_T + k_2R_V + \dfrac{1}{j2\pi fc_1}}}\right)_{\substack{0\le k_1\le 1\\ 0\le k_2\le 1}} \quad (2)$$

*Figure 11* shows the response of the circuit of *Figure 10*.

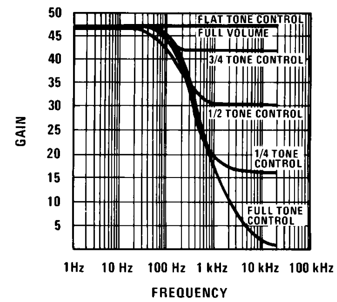


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**FIGURE 11. Tone Control Response**

Most phonograph applications require frequency response shaping to provide the RIAA equalization characteristic. When recording, the low frequencies are attenuated to prevent large undulations from destroying the record groove walls. (Bass tones have higher energy content than high frequency tones). Conversely, the high frequencies are emphasized to achieve greater signal-to-noise ratio. Therefore, when played back the phono amplifier should have the inverse frequency response as shown in *Figure 12*.

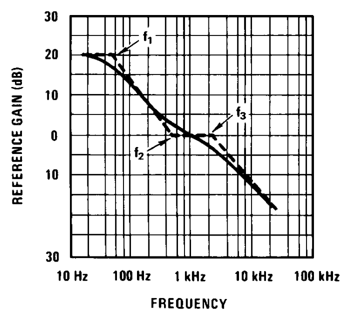


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**FIGURE 12. RIAA Playback Equalization**

This response is achieved with the circuit of *Figure 13*.

The mid-band gain, between frequencies $f_2$ and $f_3$, *Figure 12*, is established by the ratio of $R_1$ to the input resistance of the amplifier (150 kΩ).

$$\text{Mid-band Gain} = \frac{R_1 + 150\ \text{k}\Omega}{150\ \text{k}\Omega} \quad (3)$$

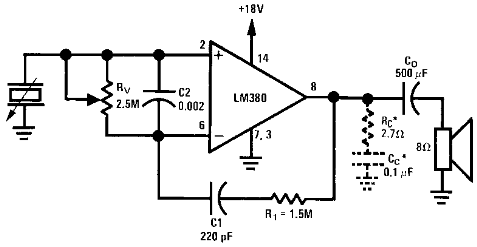


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**FIGURE 13. RIAA Phono Amplifier**

Capacitor $C_1$ sets the corner frequency $f_2$ where $R_1 = X_{C1}$.

$$C_1 = \frac{1}{2\pi f_2 R_1} \quad (4)$$

Capacitor $C_2$ establishes the corner frequency $f_3$ where $X_{C2}$ equals the impedance of the inverting input. This is normally 150 kΩ. However, in the circuit of *Figure 13* negative feedback reduces the impedance at the inverting input as:

$$Z = \frac{Z_o}{1 + A_o\beta} \quad (5)$$

Where:

$Z_o$ = impedance at node 6 without external feedback (150 kΩ)

$A_o$ = gain without external feedback (50)

$\beta$ = feedback transfer function $\beta = \dfrac{A_o - A}{A_o A}$

A = closed loop gain with external feedback.

Therefore

$$C_2 = \frac{1}{2\pi f_3 \left(\dfrac{Z_o}{1 + A_o\beta}\right)} = \frac{1}{2\pi f_3 \left(\dfrac{150\text{k}}{1 + 50\beta}\right)} \quad (6)$$

**BRIDGE AMPLIFIER**

Where more power is desired than can be provided with one amplifier, two amps may be used in the bridge configuration shown in *Figure 14*.

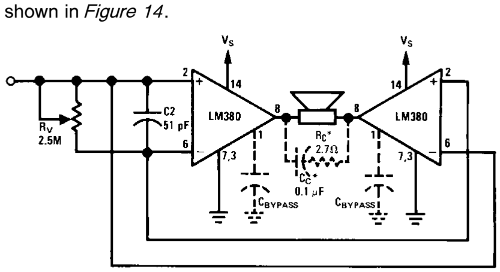


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**FIGURE 14. Bridge Configuration**

This provides twice the voltage swing across the load for a given supply, thereby, increasing the power capability by a factor of four over the single amplifier. However, in most cases the package dissipation will be the first parameter limiting power delivered to the load. When this is the case, the power capability of the bridge will be only twice that of

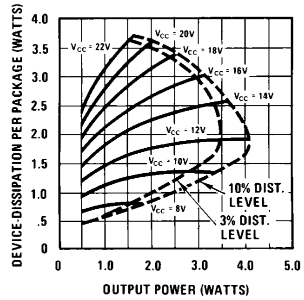


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**FIGURE 15A. 8Ω Load**

the single amplifier. *Figures 15A* and *B* show output power versus device package dissipation for both 8 and 16Ω loads in the bridge configuration. The 3% and 10% harmonic

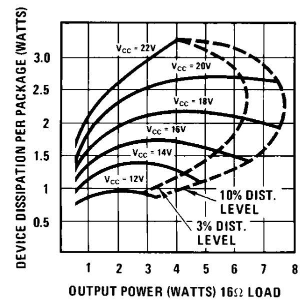


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**FIGURE 15B. 16Ω Load**

distortion contours double back due to the thermal limiting of the LM380. Different amounts of heat sinking will change the point at which the distortion contours bend.

The quiescent output voltage of the LM380 is specified at 9 ± 1 volts with an 18 volt supply. Therefore, under the worst case condition, it is possible to have two volts DC across the load.

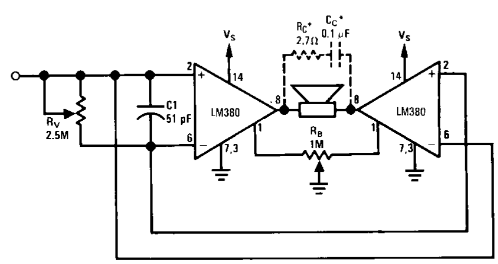


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**FIGURE 16. Quiescent Balance Control**

With an 8Ω speaker this 0.25A which may be excessive. Three alternatives are available; 1) care can be taken to match the quiescent voltages, 2) a non-polar capacitor may be placed in series with the load, 3) the offset balance control of *Figure 16* may be used.

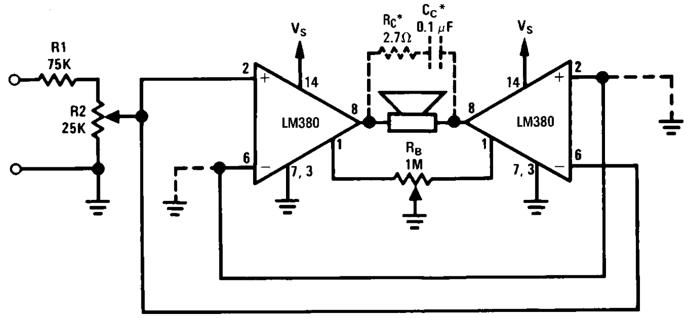


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**FIGURE 17. Voltage Divider Input**

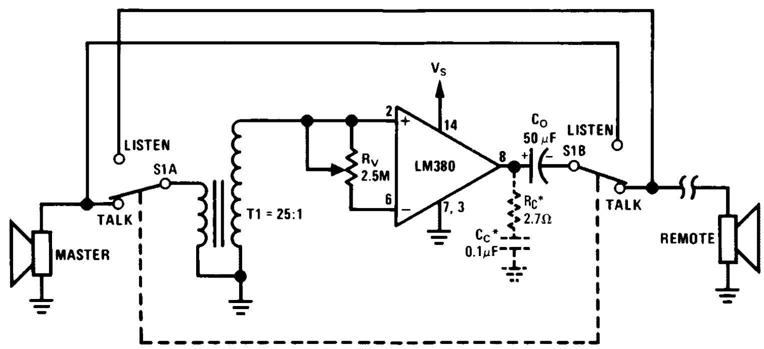


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**FIGURE 18. Intercom**

The circuits of *Figures 14* and *16* employ the "common mode" volume control as shown before. However, any of the various input connection schemes discussed previously may be used. *Figure 17* shows the bridge configuration with the voltage divider input. As discussed in the "Biasing" section the undriven input may be AC or DC grounded. If $V_S$ is an appreciable distance from the power supply (>3″) filter capacitor it should be decoupled with a 1 μF tantaulum capacitor.

### INTERCOM

The circuit of *Figure 18* provides a minimum component intercom. With switch $S_1$ in the talk position, the speaker of the master station acts as the microphone with the aid of step-up transformer $T_1$.

A turns ratio of 25 and a device gain of 50 allows a maximum loop gain of 1250. $R_V$ provides a "common mode" volume control. Switching $S_1$ to the listen position reverses the role of the master and remote speakers.

### LOW COST DUAL SUPPLY

The circuit shown in *Figure 19* demonstrates a minimum parts count method of symmetrically splitting a supply voltage. Unlike the normal R, C, and power zener diode tech-

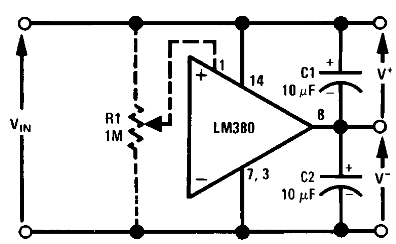


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**FIGURE 19. Dual Supply**

nique the LM380 circuit does not require a high standby current and power dissipation to maintain regulation.

With a 20 volt input voltage (±10 volt output) the circuit exhibits a change in output voltage of approximately 2% per 100 mA of unbalanced load change. Any balanced load change will reflect only the regulation of the source voltage $V_{IN}$.

The theoretical plus and minus output tracking ability is 100% since the device will provide an output voltage at one-half of the instantaneous supply voltage in the absence of a capacitor on the bypass terminal. The actual error in tracking will be directly proportional to the unbalance in the quiescent output voltage. An optional potentiometer may be placed at pin 1 as shown in *Figure 19* to null output offset. The unbalanced current output for the circuit of *Figure 18* is limited by the power dissipation of the package.

In the case of sustained unbalanced excess loads, the device will go into thermal limiting as the temperature sensing circuit begins to function. For instantaneous high current loads or short circuits the device limits the output current to approximately 1.3 amperes until thermal shut-down takes over or until the fault is removed.

**HIGH INPUT IMPEDANCE CIRCUIT**

The junction FET isolation circuit shown in *Figure 20* raises the input impedance to 22 MΩ for low frequency input signals. The gate to drain capacitance (2 pF maximum for the KE4221 shown) of the FET limits the input impedance as frequency increases.

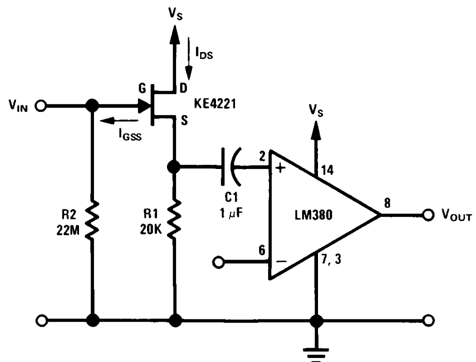


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**FIGURE 20**

At 20 kHz the reactance of this capacitor is approximately −j4 MΩ giving a net input impedance magnitude of 3.9 MΩ. The values chosen for $R_1$, $R_2$ and $C_1$ provide an overall circuit gain of at least 45 for the complete range of parameters specified for the KE4221.

When using another FET device the relevant design equations are as follows:

$$A_V = \left(\frac{R_1}{R_1 + \dfrac{1}{g_m}}\right)(50) \tag{7}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{8}$$

$$V_{GS} = I_{DS}R_1 \tag{9}$$

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{10}$$

The maximum value of $R_2$ is determined by the product of the gate reverse leakage $I_{GSS}$ and $R_2$. This voltage should be 10 to 100 times smaller than $V_P$. The output impedance of the FET source follower is:

$$R_o = \frac{1}{g_m} \tag{11}$$

so that the determining resistance for the interstage RC time constant is the input resistance of the LM380.

**BOOSTED GAIN USING POSITIVE FEEDBACK**

For applications requiring gains higher than the internally set gain of 50, it is possible to apply positive feedback around the LM380 for closed loopgains of up to 300. *Figure 21* shows a practical example of an LM380 in a gain of 200 circuit.

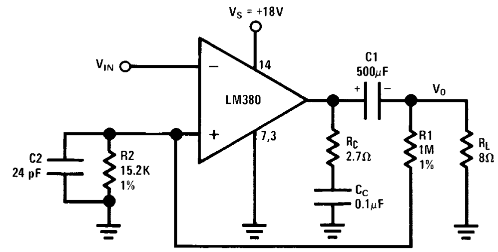


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**FIGURE 21. Boosted Gain of 200 Using Positive Feedback**

The equation describing the closed loop gain is:

$$A_{VCL} = \frac{-A_{V(\omega)}}{1 - \dfrac{A_{V(\omega)}}{1 + \dfrac{R_1}{R_2}}} \tag{12}$$

where $A_{V(\omega)}$ is complex at high frequencies but is nominally the 40 to 60 specified on the data sheet for the pass band of the amplifier. If $1 + R_1/R_2$ approaches the value of $A_{V(\omega)}$, the denominator of equation 12 approaches zero, the closed loop gain increases toward infinity, and the circuit oscillates. This is the reason for limiting the closed loop gain values to 300 or less. *Figure 22* shows the loaded and unloaded bode plot for the circuit shown in *Figure 21*.

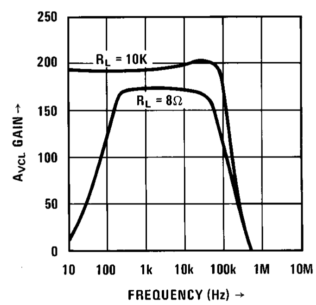


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**FIGURE 22. Boosted Gain Bode Plot**

The 24 pF capacitor $C_2$ shown on *Figure 21* was added to give an overdamped square wave response under full load conditions. It causes a high frequency roll-off of:

$$f_2 = \frac{1}{2\pi R_2 C_2} \tag{13}$$

The circuit of *Figure 21* will have a very long (1000 sec) turn on time if $R_L$ is not present, but only a 0.01 second turn on time with an 8Ω load.

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