

# CMOS Dual 64-Stage Static Shift Register

# CD4517B Types

High-Voltage Types (20-Volt Rating)

■ CD4517B dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the CD4517B. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

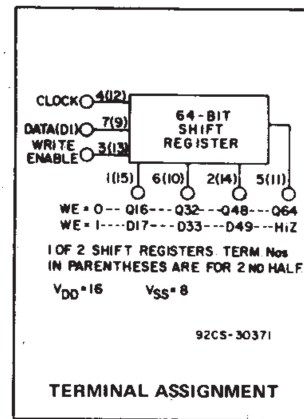
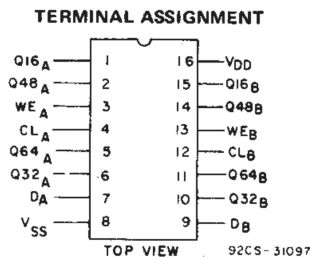
The CD4517B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**Features:**

- Low quiescent current – 10 nA/pkg (typ.) at  $V_{DD} = 5V$
- Clock frequency 12 MHz (typ.) at  $V_{DD} = 10V$
- Schmitt trigger clock inputs allow operation with very slow clock rise and fall times
- Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads
- Three-state outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

**Applications:**

- Time-delay circuits
- Scratch-pad memories
- General-purpose serial shift-register applications



**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{mA}$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max	$+265^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$ )	3	18	V

**TRUTH TABLE**

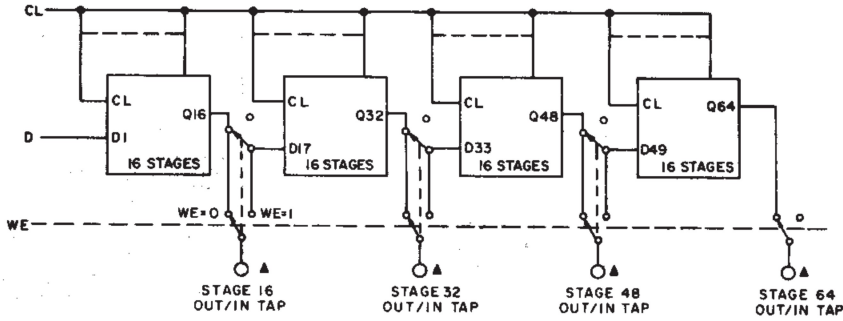
Clock	Write Enable	Data	Stage 16 Tap	Stage 32 Tap	Stage 48 Tap	Stage 64 Tap
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
1	0	DI In	Q16	Q32	Q48	Q64
1	1	DI In	D17 In	D33 In	D49 In	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z

X = Don't Care

Z = High Impedance

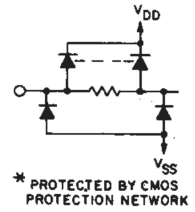
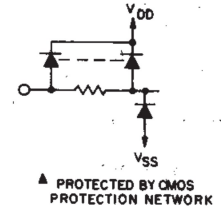
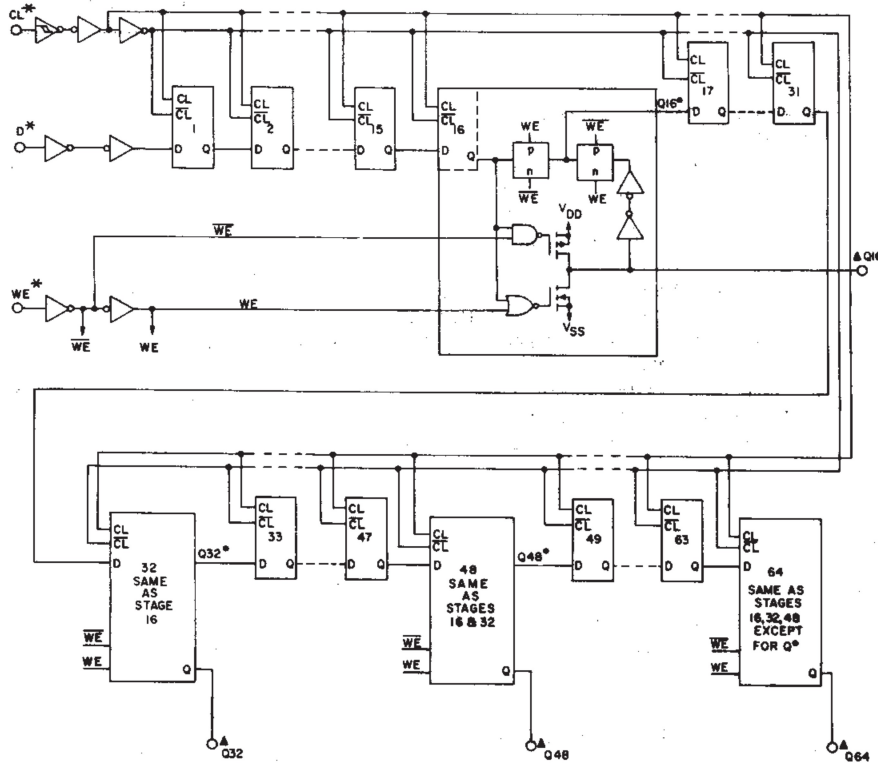
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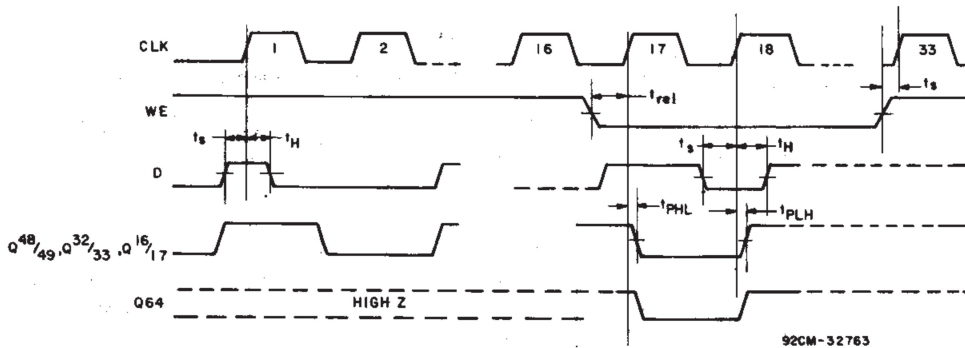
92CM-31098R1

Fig. 1—CD4517B functional block diagram (one half).



92CL-32765

Fig. 2—CD4517B logic block diagram (one half).



92CM-32763

Fig. 3—Dynamic test waveforms.

# CD4517B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0,5	5	0,05			-	0	0,05	-	V
	-	0,10	10	0,05			-	0	0,05	-	
	-	0,15	15	0,05			-	0	0,05	-	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0,5	5	4,95			4,95	5	-	-	V
	-	0,10	10	9,95			9,95	10	-	-	
	-	0,15	15	14,95			14,95	15	-	-	
Input Low Voltage V <sub>IL</sub> Max.	0,5, 4,5	-	5	1,5			-	-	1,5	-	V
	1,9	-	10	3			-	-	3	-	
	1,5, 13,5	-	15	4			-	-	4	-	
Input High Voltage V <sub>IH</sub> Min.	0,5, 4,5	-	5	3,5			3,5	-	-	-	V
	1,9	-	10	7			7	-	-	-	
	1,5, 13,5	-	15	11			11	-	-	-	
Input Current I <sub>IN</sub> Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	μA
3-State Output Leakage Current I <sub>OUT</sub> Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	-	±10 <sup>-4</sup>	±0,4	μA

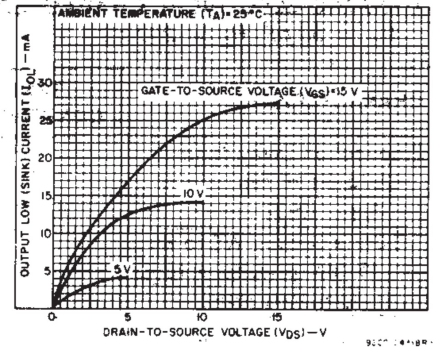


Fig. 4—Typical n-channel output low (sink) current characteristics.

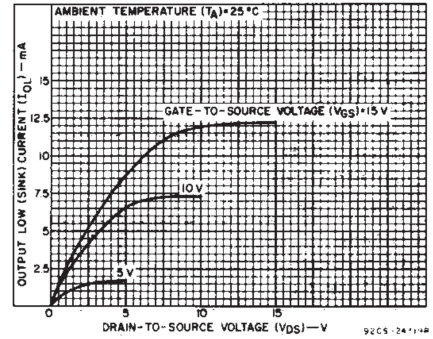


Fig. 5—Minimum n-channel output low (sink) current characteristics.

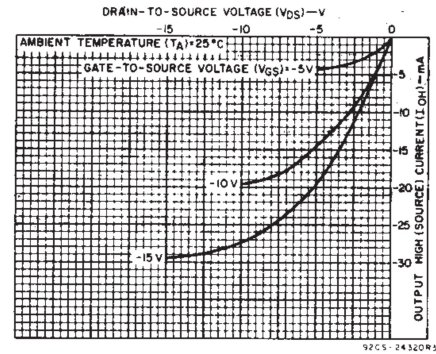


Fig. 6—Typical p-channel output high (source) current characteristics.

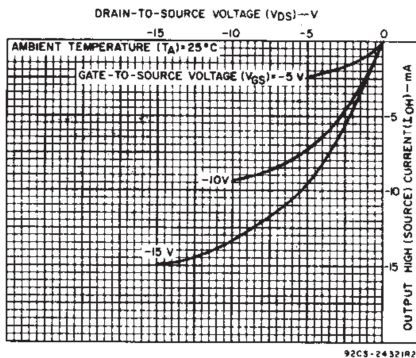


Fig. 7—Minimum p-channel output high (source) current characteristics.

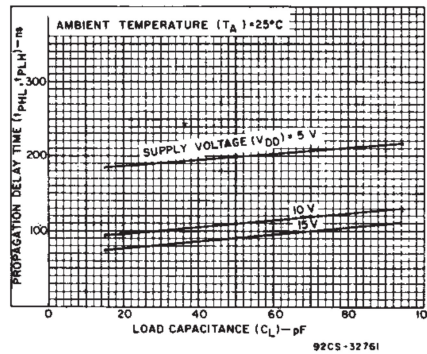


Fig. 8—Typical propagation delay time as a function of load capacitance.

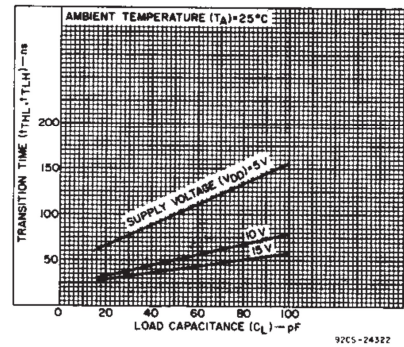


Fig. 9—Typical transition time as a function of load capacitance.

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**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	V <sub>DD</sub> (V)	LIMITS			UNITS
			Min.	Typ.	Max.	
Propagation Delay Time: CL to Bit 16 Tap $t_{PHL}, t_{PLH}$		5	—	200	400	ns
		10	—	110	220	
		15	—	90	180	
3-State Output, WE to Bit 16 Tap $t_{PHZ}, t_{PLZ}; t_{PZH}, t_{PZL}$ (See Note)		5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
Output Transition Time $t_{THL}, t_{TLH}$		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Write Enable-to-Clock Setup Time		5	0	-50	—	ns
		10	0	-25	—	
		15	0	-15	—	
Data-to-Clock Setup Time, $t_s$		5	20	0	—	ns
		10	10	0	—	
		15	10	0	—	
Minimum Write Enable-to-Clock Release Time		5	—	50	100	ns
		10	—	25	50	
		15	—	20	40	
Minimum Data-to-Clock Hold Time, $t_H$		5	—	100	200	ns
		10	—	50	100	
		15	—	25	50	
Minimum Clock Pulse Width, $t_W$		5	—	90	180	ns
		10	—	40	80	
		15	—	25	50	
Maximum Clock Input Frequency, $f_{CL}$		5	3	6	—	MHz
		10	6	12	—	
		15	8	15	—	
Maximum Clock Input Rise or Fall Time, $t_{fCL}, t_{rCL}$		5	UNLIMITED			$\mu\text{s}$
		10	UNLIMITED			
		15	UNLIMITED			
Input Capacitance $C_{iN}$	Any Input		—	5	7.5	pF

**NOTE:** Measured at the point of 10% change in output with an output load of 50 pF,  $R_L = 1\text{ k}\Omega$  to  $V_{DD}$  for  $t_{PZL}, t_{PLZ}$  and  $R_L = 1\text{ k}\Omega$  to  $V_{SS}$  for  $t_{PZH}, t_{PHZ}$ .

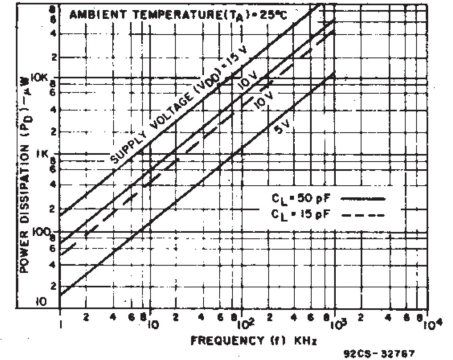


Fig. 10—Typical power dissipation as a function of frequency.

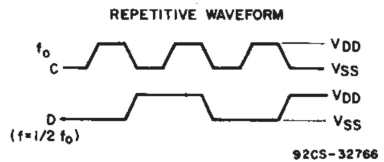
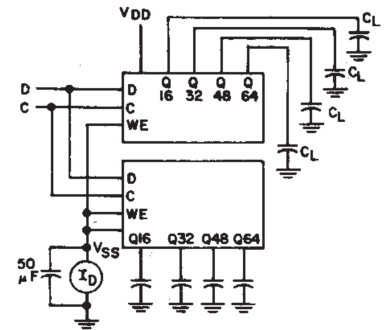


Fig. 11—Dynamic power dissipation test circuit and waveforms.

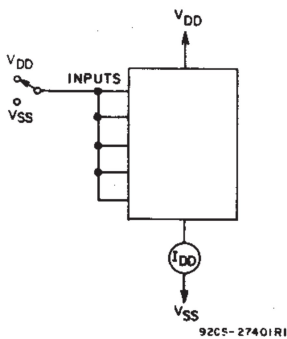


Fig. 12—Quiescent device current test circuit.

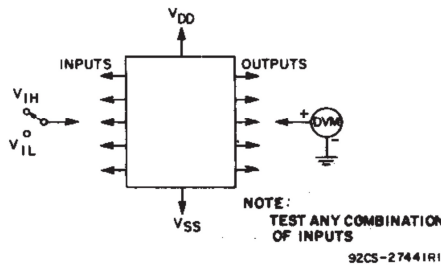


Fig. 13—Input voltage test circuit.

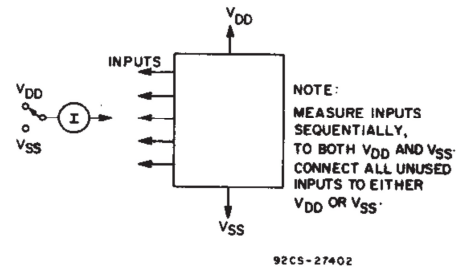
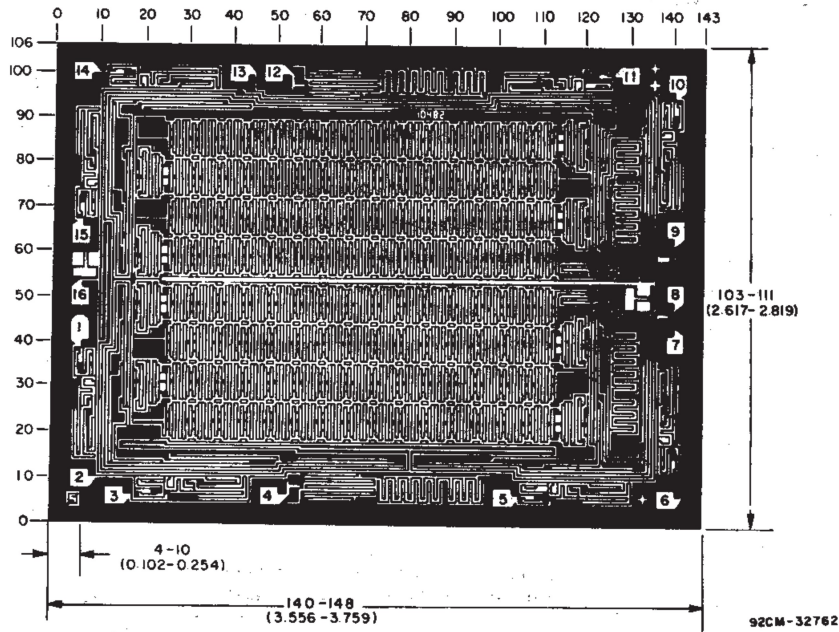


Fig. 14—Input current test circuit.

# CD4517B Types



*Dimensions and pad layout for CD4517B.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

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