CD4069UB CMOS Hex Inverter

1 Features

- Standardized Symmetrical Output Characteristics
- Medium Speed Operation: $-t_{PHL}$, t_{PLH} = 30 ns at 10 V (Typical)
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 µA at 18 V Over Full Package-Temperature Range, 100 nA at 18 V and 25°C
- Meets All Requirements of JEDEC Tentative Standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*

2 Applications

- Logic Inversion
- Pulse Shaping
- Oscillators
- High-Input-Impedance Amplifiers

3 Description

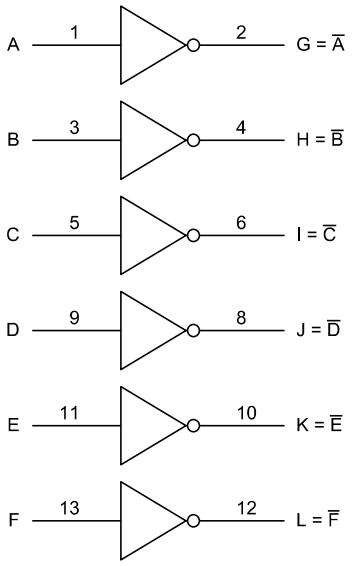
The CD4069UB device consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 hex inverter and buffers are not required.

Device Information(1)

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
CD4069UBE	PDIP (14)	19.30 mm × 6.35 mm
CD4069UBF	CDIP (14)	19.56 mm × 6.67 mm
CD4069UBM	SOIC (14)	8.65 mm × 3.91 mm
CD4069UBNSR	SO (14)	10.30 mm × 5.30 mm
CD4069UBPW	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

CD4069UB Functional Diagram



V_{DD} = Pin 14
V_{SS} = Pin 7

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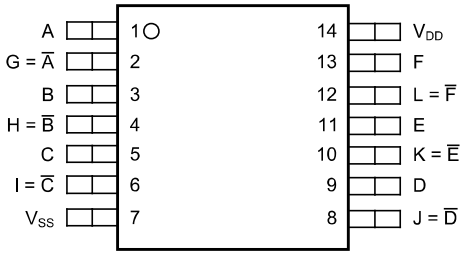
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2003) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D, J, N, NS, and PW Packages
14-Pin PDIP, CDIP, SOIC, SO, and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	A input
B	3	I	B input
C	5	I	C input
D	9	I	D input
E	11	I	E input
F	13	I	F input
G = $\overline{A}$	2	O	G output
H = $\overline{B}$	4	O	H output
I = $\overline{C}$	6	O	I output
J = $\overline{D}$	8	O	J output
K = $\overline{E}$	10	O	K output
L = $\overline{F}$	12	O	L output
V_{DD}	14	—	Positive supply
V_{SS}	7	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	DC supply-voltage (voltages referenced to V_{SS} terminal)		–0.5	20	V
V_I	Input voltage, all inputs		–0.5 to V_{DD}	0.5	V
I_{IK}	DC input current, any one input		–10	10	mA
P_D	Power dissipation per package	–55°C to 100°C		500	mW
		100°C to 125°C	12	200	
	Device dissipation per output transistor	Full range (all package types)		100	mW
	Lead temperature(2)			265	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) During soldering at distance 1/16 inch ± 1/32 inch (1.59 mm ± 0.79 mm) from case for 10 s maximum

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		CD4069UB					UNIT
		D (SOIC)	J (CDIP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	—	57.9	91.2	122.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	28.5	45.5	48.8	50.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.2	—	37.7	50	63.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.1	—	30.6	15	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	—	37.6	49.6	63.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – Dynamic

T_A = 25°C; input t_r, t_f = 20 ns; C_L = 50 pF; R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	V_{DD} (V) = 5		55	110	ns
		V_{DD} (V) = 10		30	60	
		V_{DD} (V) = 15		25	50	
t_{THL}, t_{TLH}	Transition time	V_{DD} (V) = 5		100	200	ns
		V_{DD} (V) = 10		50	100	
		V_{DD} (V) = 15		40	80	
C_{IN}	Input capacitance	Any input		10	15	pF

6.6 Electrical Characteristics – Static

T_A = 25°C; input t_r, t_f = 20 ns; C_L = 50 pF; R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}max	Quiescent device current	V_{IN} = 0V or 5 V , V_{DD} = 5 V	T_A = –55°C			0.25	µA
			T_A = –40°C			0.25	
			T_A = 25°C		0.01	0.25	
			T_A = 85°C			7.5	
			T_A = 125°C			7.5	
		V_{IN} = 0 or 10 V, V_{DD} = 10 V	T_A = –55°C			0.5	
			T_A = –40°C			0.5	
			T_A = 25°C		0.01	0.5	
			T_A = 85°C			15	
			T_A = 125°C			15	
		V_{IN} = 0 or 15 V, V_{DD} = 15 V	T_A = –55°C			1	
			T_A = –40°C			1	
			T_A = 25°C		0.01	1	
			T_A = 85°C			30	
			T_A = 125°C			30	
		V_{IN} = 0 or 20 V, V_{DD} = 20 V	T_A = –55°C			5	
			T_A = –40°C			5	
			T_A = 25°C		0.02	5	
			T_A = 85°C			150	
			T_A = 125°C			150	
I_{OL}min	Output low (sink) current	V_O = 0.4 V, V_{IN} = 5 V, V_{DD} = 5 V	T_A = –55°C	0.64			mA
			T_A = –40°C	0.61			
			T_A = 25°C	0.51	1		
			T_A = 85°C	0.42			
			T_A = 125°C	0.36			
		V_O = 0.5 V, V_{IN} = 10 V, V_{DD} = 10 V	T_A = –55°C	1.6			
			T_A = –40°C	1.5			
			T_A = 25°C	1.3	2.6		
			T_A = 85°C	1.1			
			T_A = 125°C	0.9			
		V_O = 1.5 V, V_{IN} = 15 V, V_{DD} = 15 V	T_A = –55°C	4.2			
			T_A = –40°C	4			
			T_A = 25°C	3.4	6.8		
			T_A = 85°C	2.8			
			T_A = 125°C	2.4			

Electrical Characteristics – Static (continued)

T_A = 25°C; input t_r, t_f = 20 ns; C_L = 50 pF; R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OH}min	Output high (source) current	V_O = 4.6 V, V_{IN} = 0 V, V_{DD} = 5 V	T_A = –55°C	–0.64			mA
			T_A = –40°C	–0.61			
			T_A = 25°C	–0.51	–1		
			T_A = 85°C	–0.42			
			T_A = 125°C	–0..36			
		V_O = 2.5 V, V_{IN} = 0 V, V_{DD} = 5 V	T_A = –55°C	–2			
			T_A = –40°C	–1.8			
			T_A = 25°C	–1.6	–3.2		
			T_A = 85°C	–1.3			
			T_A = 125°C	–1.15			
		V_O = 9.5 V, V_{IN} = 0 V, V_{DD} = 10 V	T_A = –55°C	–1.6			
			T_A = –40°C	–1.5			
			T_A = 25°C	–1.3	–2.6		
			T_A = 85°C	–1.1			
			T_A = 125°C	–0.9			
		V_O = 13.5 V, V_{IN} = 0 V, V_{DD} = 15 V	T_A = –55°C	–4.2			
			T_A = –40°C	–4			
			T_A = 25°C	–3.4	–6.8		
			T_A = 85°C	–2.8			
			T_A = 125°C	–2.4			
V_{OL}max	Low-level output voltage	V_{IN} = 5 V, V_{DD} = 5 V	T_A = 25°C		0	0.05	V
			All other temperatures			0.05	
		V_{IN} = 10 V, V_{DD} = 10 V	T_A = 25°C		0	0.05	
			All other temperatures			0.05	
		V_{IN} = 15 V, V_{DD} = 15 V	T_A = 25°C		0	0.05	
			All other temperatures			0.05	
V_{OH}min	High-level output voltage	V_{IN} = 0 V, V_{DD} = 5 V	T_A = 25°C	4.95	5		V
			All other temperatures	4.95			
		V_{IN} = 0 V, V_{DD} = 10 V	T_A = 25°C	9.95	10		
			All other temperatures	9.95			
		V_{IN} = 0 V, V_{DD} = 15 V	T_A = 25°C	14.95	15		
			All other temperatures	14.95			
V_{IL}max	Input low voltage	V_O = 4.5 V, V_{DD} = 5 V, all temperatures				1	V
		V_O = 9 V, V_{DD} = 10 V, all temperatures				2	
		V_O = 13.5 V, V_{DD} = 15 V, all temperatures				2.5	
V_{IH}min	Input high voltage	V_O = 0.5 V, V_{DD} = 5 V, all temperatures		4			V
		V_O = 1 V, V_{DD} = 10 V, all temperatures		8			
		V_O = 1.5 V, V_{DD} = 15 V, all temperatures		12.5			

Electrical Characteristics – Static (continued)

T_A = 25°C; input t_r, t_f = 20 ns; C_L = 50 pF; R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IN}max	Input current	V_{IN} = 0 V to 18 V, V_{DD} = 18 V	T_A = –55°C			±01	µA
			T_A = –40°C			±01	
			T_A = 25°C		$±10^{-5}$	±1	
			T_A = 85°C			±1	
			T_A = 125°C			±1	

6.7 Typical Characteristics

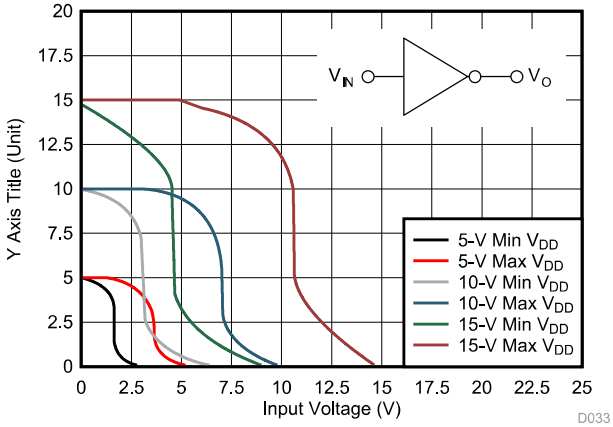


Figure 1. Minimum and Maximum Voltage Transfer Characteristics

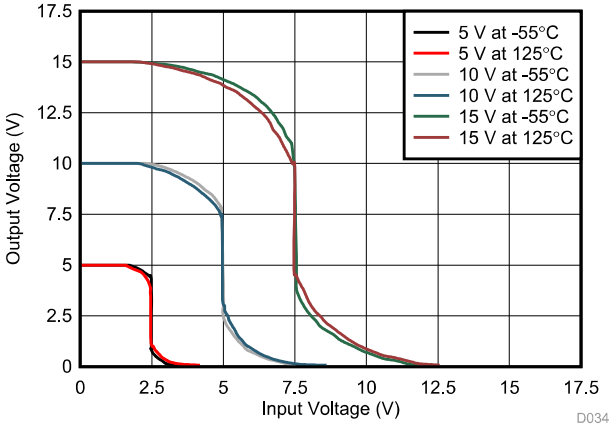


Figure 2. Typical Voltage Transfer Characteristics as a Function of Temperature

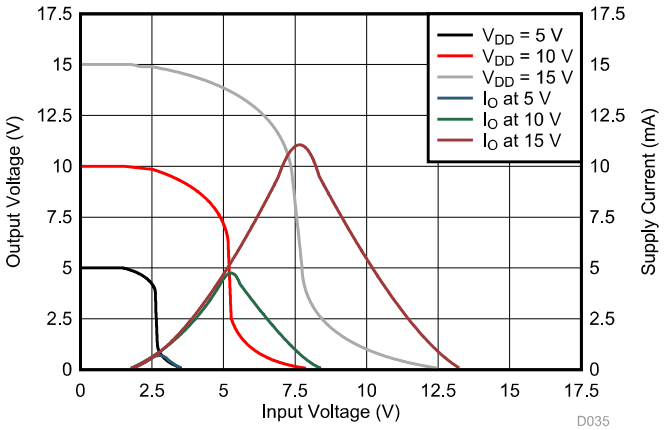


Figure 3. Typical Current and Voltage Transfer Characteristics

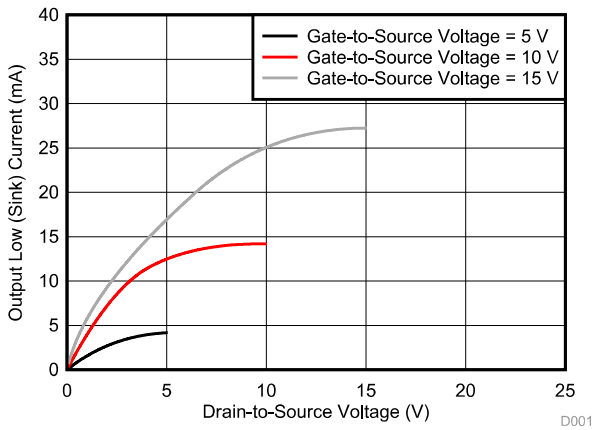


Figure 4. Typical Output Low (Sink) Current Characteristics

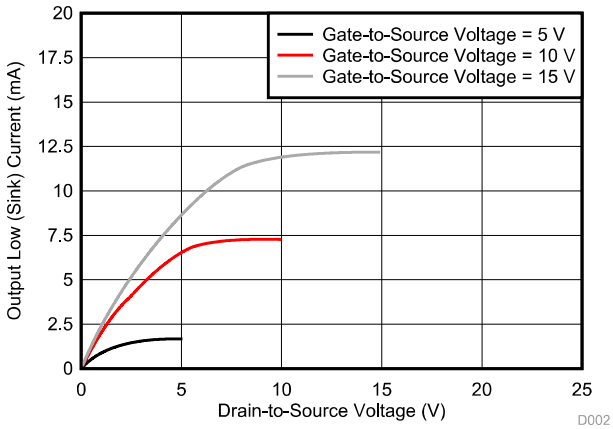


Figure 5. Minimum Output Low (Sink) Current Characteristics

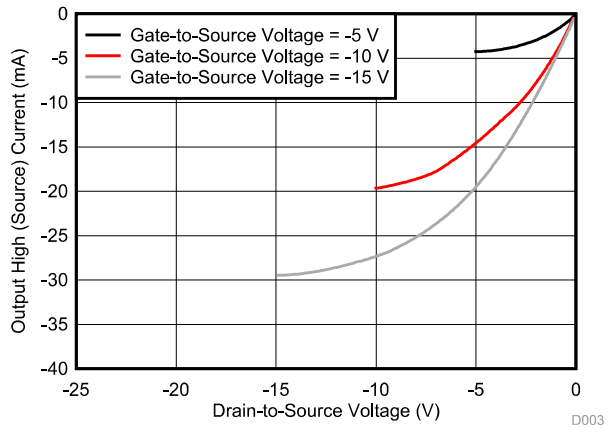


Figure 6. Typical Output High (Source) Current Characteristics

Typical Characteristics (continued)

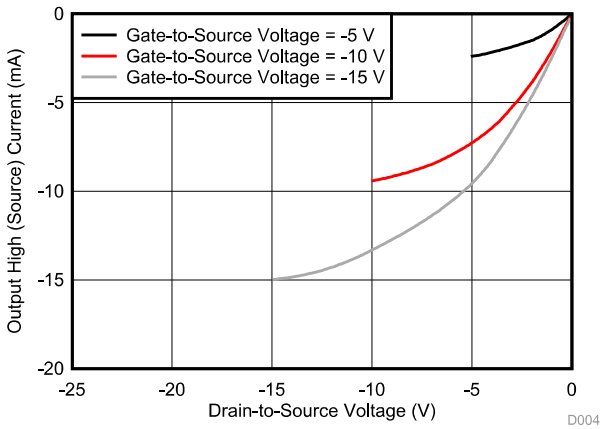


Figure 7. Minimum Output High (Source) Current Characteristics

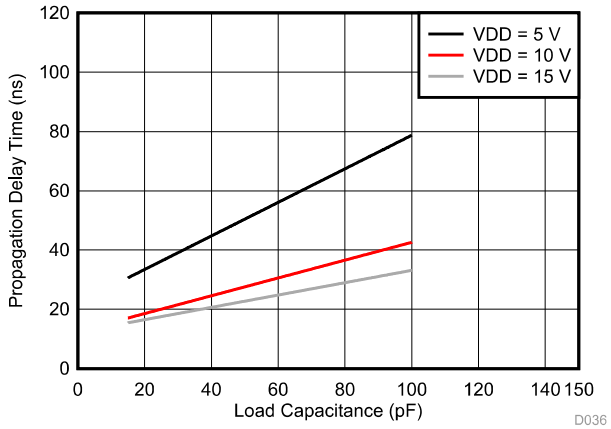


Figure 8. Typical Propagation Delay Time vs Load Capacitance

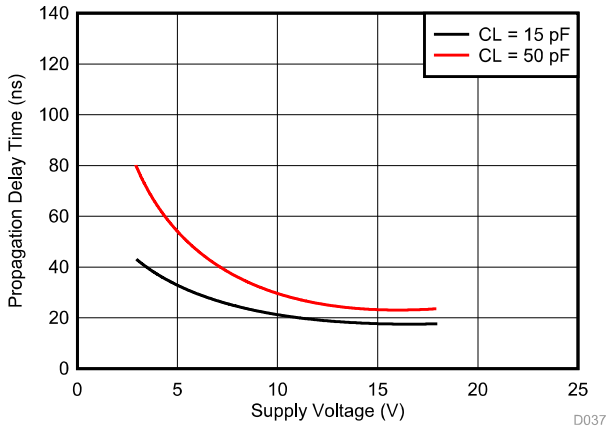


Figure 9. Typical Propagation Delay Time vs Supply Voltage

7 Parameter Measurement Information

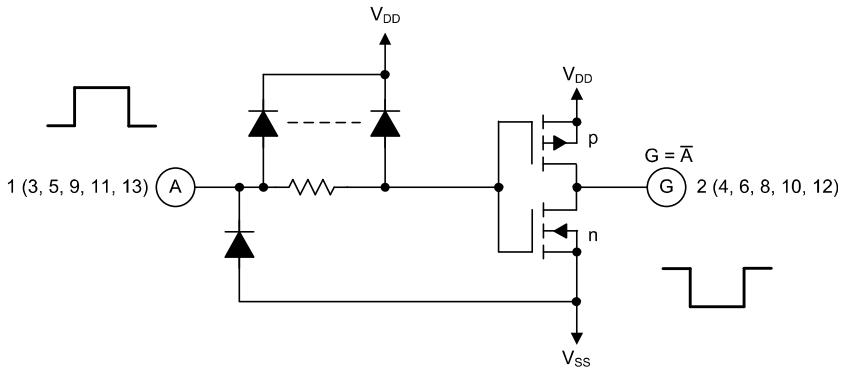


Figure 10. Schematic Diagram of One of Six Identical Inverters

Parameter Measurement Information (continued)

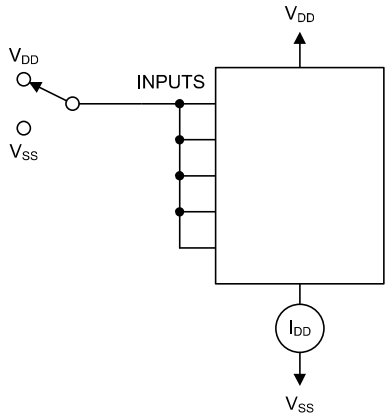


Figure 11. Quiescent Device Current Test Circuit

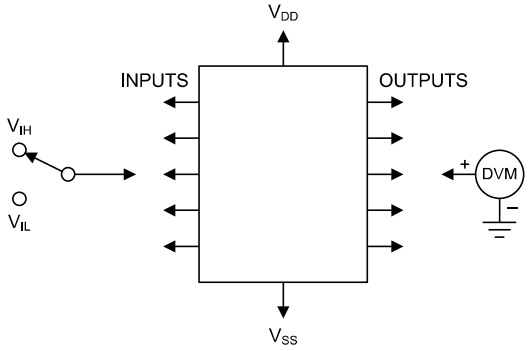


Figure 12. Noise Immunity Test Circuit

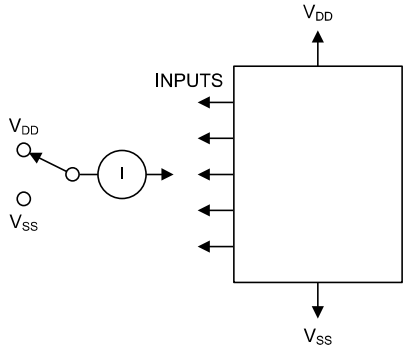


Figure 13. Input Leakage Current Test Circuit

Parameter Measurement Information (continued)

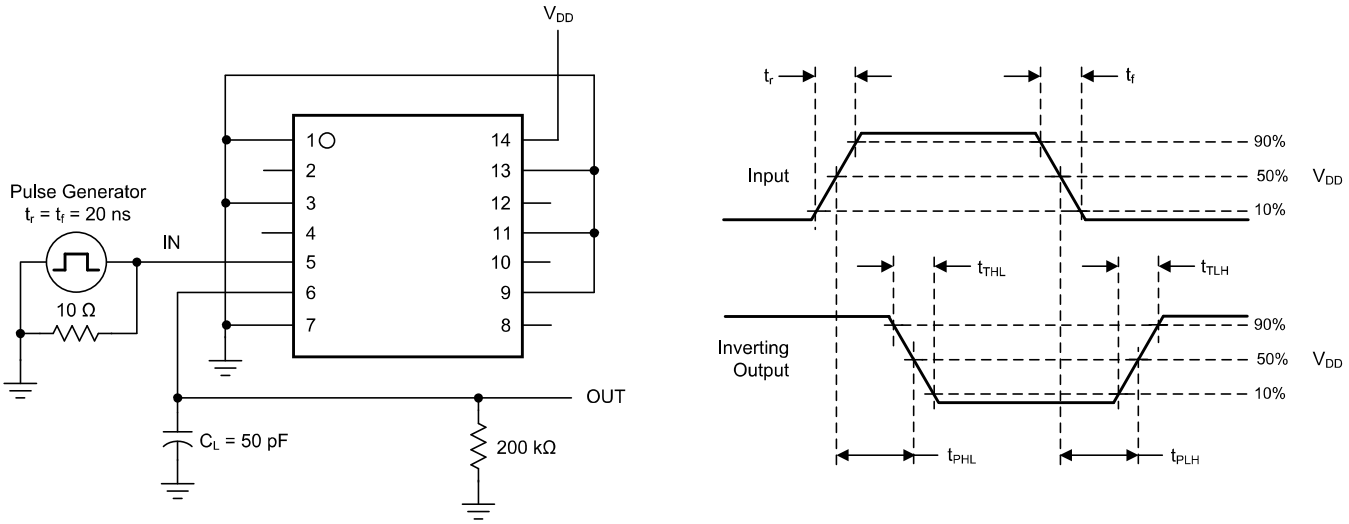


Figure 14. Dynamic Electrical Characteristics Test Circuit and Waveform

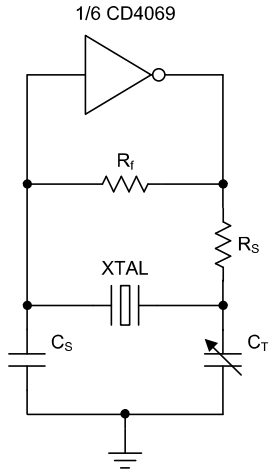


Figure 15. Typical Crystal Oscillator Circuit

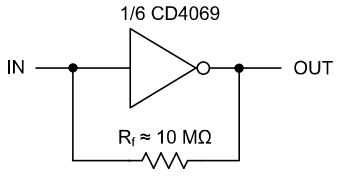


Figure 16. High-Input Impedance Amplifier

Parameter Measurement Information (continued)

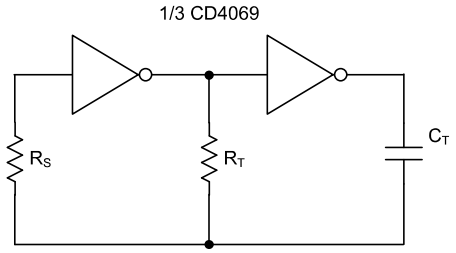
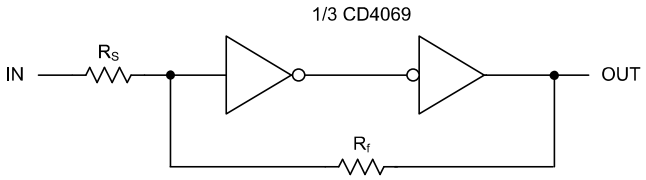


Figure 17. Typical RC Oscillator Circuit



Upper Switching Point :

$$V_P = \frac{R_S + R_f}{R_f} \times \frac{V_{DD}}{2}$$

Lower Switching Point :

$$V_N = \frac{R_f - R_S}{R_f} \times \frac{V_{DD}}{2}$$

$$R_f > R_S$$

Figure 18. Input Pulse Shaping Circuit

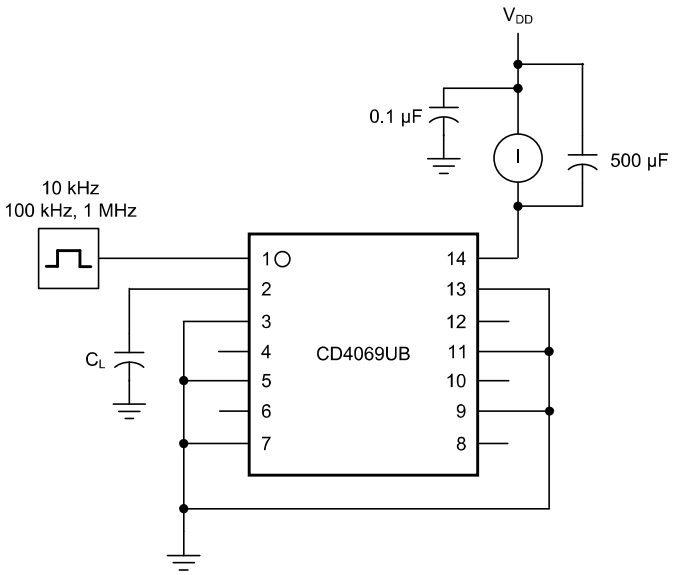


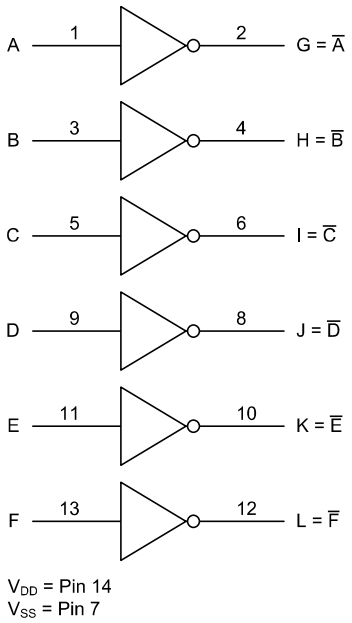
Figure 19. Dynamic Power Dissipation Test Circuit

8 Detailed Description

8.1 Overview

The CD4069UB device has six inverter circuits. The recommended operating range is from 3 V to 18 V. The CD4069UB-series types are supplied in 14-pin hermetic dual-in-line ceramic packages (F3A suffix), 14-pin dual-in-line plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

8.2 Functional Block Diagram



8.3 Feature Description

CD4069UB has standardized symmetrical output characteristics and a wide operating voltage range from 3 V to 18 V with quiescent current tested at 20 V. This has a medium operation speed –t_{PHL}, t_{PLH} = 30 ns (typical) at 10 V. The operating temperature is from –55°C to 125°C. CB4069B meets all requirements of JEDEC tentative standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*.

8.4 Device Functional Modes

Table 1 shows the functional modes for CD4069UB.

Table 1. Function Table

INPUT A, B, C, D, E, F	OUTPUT G, H, I, J, K, L
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CD4069UB device has a low input current of 1 µA at 18 V over full package-temperature range and 100 nA at 18 V, 25°C. This device has a wide operating voltage range from 3 V to 18 V and used in high voltage applications.

9.2 Typical Application

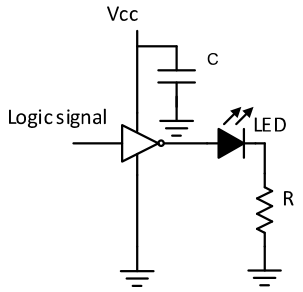


Figure 20. CD4069UB Application

9.2.1 Design Requirements

The CD4069UB device is the industry's highest logic inverter operating at 18 V under recommended conditions. The lower drive capabilities makes it suitable for driving light loads like LED and greatly reduces chances of overshoots and undershoots.

9.2.2 Detailed Design Procedure

The recommended input conditions for Figure 20 includes rise time and fall time specifications (see Δt/ΔV in *Recommended Operating Conditions*) and specified high and low levels (see V_{IH} and V_{IL} in *Recommended Operating Conditions*). Inputs are not overvoltage tolerant and must be below V_{CC} level because of the presence of input clamp diodes to V_{CC}.

The recommended output condition for the CD4069UB application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through V_{CC} or GND) for the device. These limits are located in the *Absolute Maximum Ratings*. Outputs must not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curves

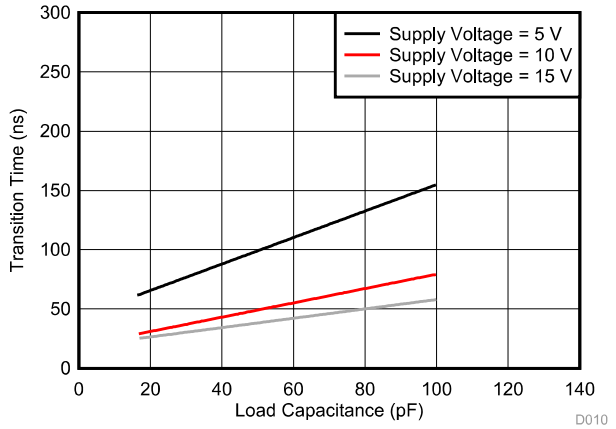


Figure 21. Typical Transition Time vs Load Capacitance

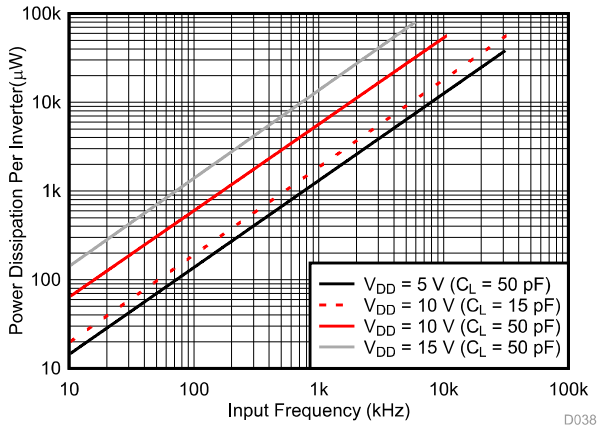


Figure 22. Typical Dynamic Power Dissipation vs Frequency

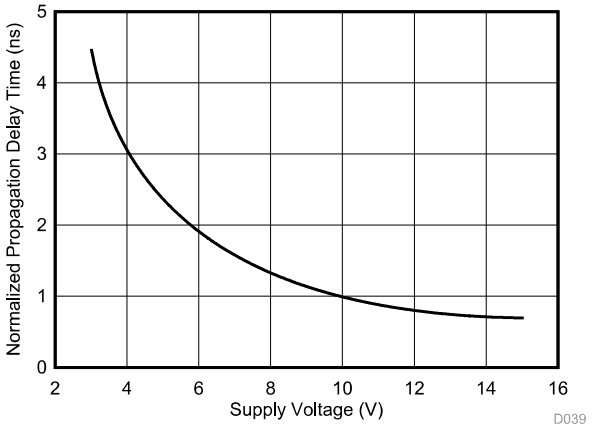


Figure 23. Variation of Normalized Propagation Delay Time (t_{PHL} and t_{PLH}) With Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple V_{CC} pins, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

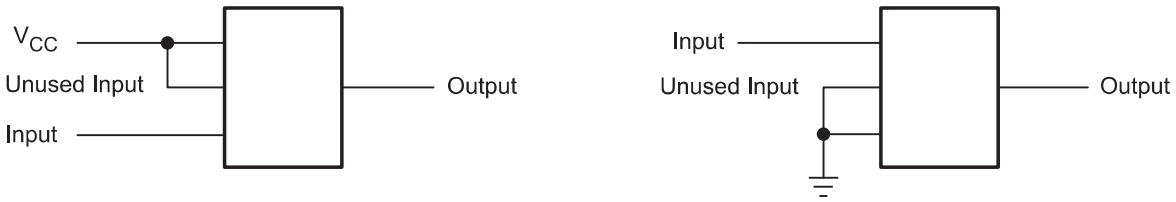
11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See the application note, *Implications of Slow or Floating CMOS Inputs* (SCBA004), for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or V_{CC} (whichever is convenient).

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.