

SN5450, SN7450

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

SDLS112 - DECEMBER 1983 - REVISED MARCH 1988

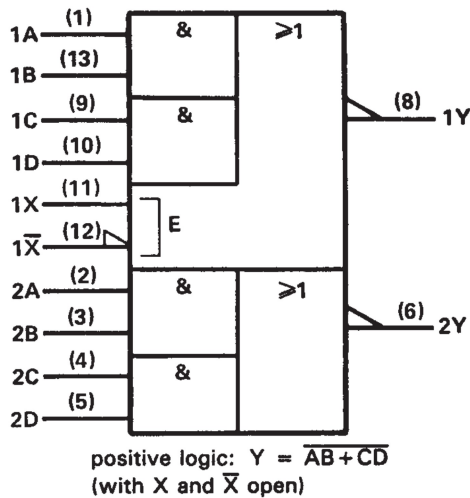
- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 2-wide 2-input AND-OR-INVERT gates with one gate expandable. They perform the Boolean function $Y = \overline{AB + CD}$ with X and \overline{X} left open.

The SN5450 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7450 is characterized for operation from 0°C to 70°C .

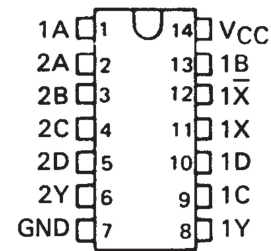
logic symbol†



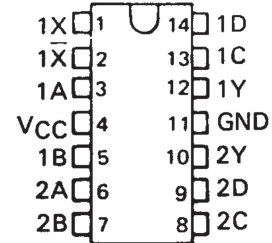
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

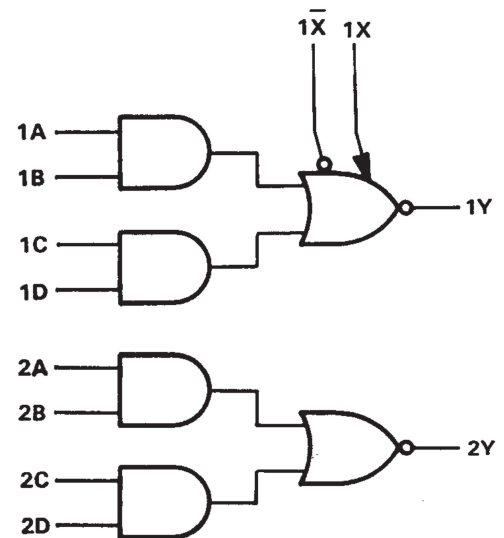
SN5450 . . . J PACKAGE
SN7450 . . . N PACKAGE
(TOP VIEW)



SN5450 . . . W PACKAGE
(TOP VIEW)



logic diagram (positive logic)



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recommended operating conditions

	SN5450			SN7450			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5450			SN7450			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _{IH} = 2.4 V			40			40	μA
I _{IL}	V _{CC} = MAX, V _{IL} = 0.4 V			-1.6			-1.6	mA
I _{OS} §	V _{CC} = MAX	-20		-55	-18		-55	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		4	8		4	8	mA
I _{CCL}	V _{CC} = MAX, See Note 2		7.4	14		7.4	14	mA
I _X ¶	V _{XX} = 0.4 V, I _{OL} = 16 mA			-2.9			-3.1	mA
V _{BE(Q)} ¶	I _X + I _X = 0.41 mA, R _{XX} = 0, I _{OL} = 16 mA			1.1				V
	I _X + I _X = 0.62 mA, R _{XX} = 0, I _{OL} = 16 mA						1	V
V _{OH} ¶	I _X = 0.15 mA, I _X = -0.15 mA, I _{OH} = -0.4 mA	2.4	3.4					V
	I _X = 0.27 mA, I _X = -0.27 mA, I _{OH} = -0.4 mA				2.4	3.4		V
V _{OL} ¶	I _X + I _X = 0.3 mA, R _{XX} = 138 Ω, I _{OL} = 16 mA		0.2	0.4				V
	I _X + I _X = 0.43 mA, R _{XX} = 130 Ω, I _{OL} = 16 mA					0.2	0.4	V

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Using expander inputs, V_{CC} = MIN, T_A = MIN, except typical values.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 400 Ω, C _L = 15 pF Expander pins open		13	22	ns
t _{PHL}					8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

