TEXAS INSTRUMENTS

SN5407, SN5417, SN7407, SN7417

SDLS032H – DECEMBER 1983 – REVISED SEPTEMBER 2016

SNx407 and SNx417 Hex Buffers and Drivers With Open-Collector High-Voltage Outputs

1 Features

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability Design
- Open-Collector Driver for Indicator Lamps
- Inputs Fully Compatible With Most TTL Circuits
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Audio Docks: Portable
- Blu-ray Disc® Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom and Server AC or DC Supply: Single Controllers: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Servers
- Wireless Headsets, Keyboards, and Mice

3 Description

These TTL hex buffers and drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays), and also are characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 devices have minimum breakdown voltages of 30 V, and the SN5417 and SN7417 devices have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5407 and SN5417 devices and 40 mA for the SN7407 and SN7417 devices.

These devices perform the Boolean function Y = A in positive logic.

These circuits are completely compatible with most TTL families. Inputs are diode clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 145 mW, and average propagation delay time is 14 ns.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx407J, SNx417J	CDIP (14)	19.56 mm × 6.92 mm
SN74x7D	SOIC (14)	8.65 mm × 3.91 mm
SN74x7N	PDIP (14)	19.30 mm × 6.35 mm
SNJ5407FK	LCCC (20)	8.89 mm × 8.89 mm
SNJ5407W	CFP (14)	9.21 mm × 5.97 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Buffer and Driver (Positive Logic)

Table of Contents

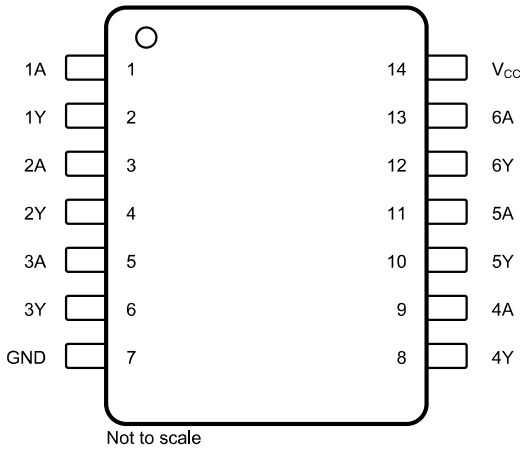
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2004) to Revision H	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table; see POA at the end of the data sheet.	1
• Added Military Disclaimer to Features	1
• Changed $R_{\theta JA}$ values for SN7404: D (SOIC) from 86 to 86.8, N (PDIP) from 80 to 52.1, and NS (SO) from 76 to 85.9	5

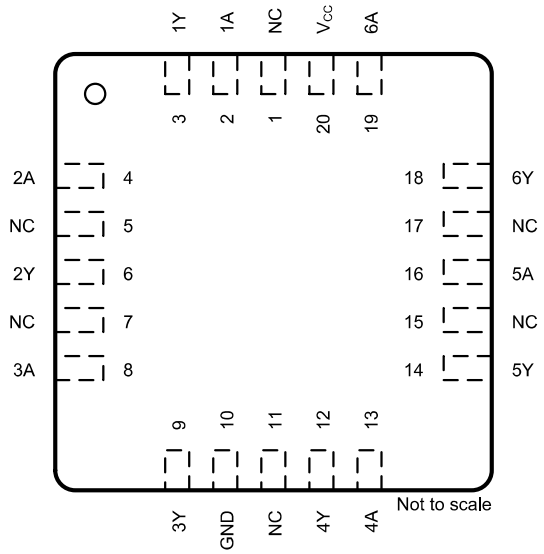
5 Pin Configuration and Functions

D, N, NS, J, or W Package
14-Pin SOIC, PDIP, CDIP, or CFP
Top View



Not to scale

FK Package
20-Pin LCCC
Top View



Not to scale

NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, PDIP, CDIP, CFP	LCCC		
1A	1	2	I	Input 1
1Y	2	3	O	Output 1
2A	3	4	I	Input 2
2Y	4	6	O	Output 2
3A	5	8	I	Input 3
3Y	6	9	O	Output 3
4A	9	13	I	Input 4
4Y	8	12	O	Output 4
5A	11	16	I	Input 5
5Y	10	14	O	Output 5
6A	13	19	I	Input 6
6Y	12	18	O	Output 6
GND	7	10	—	Ground Pin
NC	—	1, 5, 7, 11, 15, 17	—	No Connect
V_{CC}	14	20	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			7	V
V_I	Input voltage(2)			5.5	V
V_O	Output voltage(2)(3)	SN5407, SN7407		30	V
		SN5417, SN7417		15	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) This is the maximum voltage that can safely be applied to any output when it is in the OFF state.

6.2 ESD Ratings

			VALUE	UNIT
SN7407 AND SN7417				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
SN5407 AND SN5417				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN5407, SN5417	4.5	5	5.5	V
		SN7407, SN7417	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	SN5407, SN7407			30	V
		SN5417, SN7417			15	
I_{OL}	Low-level output current	SN5407, SN5417			30	mA
		SN7407, SN7417			40	
T_A	Operating free-air temperature	SN5407, SN5417	–55		125	°C
		SN7407, SN7417	0		70	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*,.

6.4 Thermal Information

THERMAL METRIC[1]		SN7407			SN7417		UNIT
		D (SOIC)	N (PDIP)	NS (SO)	D (SOIC)	N (PDIP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	86.8	52.1	85.9	88.8	52.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.1	39.4	43.9	50.4	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41	32	44.7	43	32	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.6	24.2	14.6	16.5	24.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.8	31.8	44.4	42.8	31.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –12 mA				–1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	I_{OL} = 16 mA			0.4	V
			I_{OL} = 30 mA, SN5407, SN5417			0.7	
			I_{OL} = 40 mA, SN7407, SN7417			0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V	V_{OH} = 30 V, SN5407, SN7407			0.25	mA
			V_{OH} = 15 V, SN5417, SN7417			0.25	
I_I	Input current	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_{IH} = 2.4 V				40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_{IL} = 0.4 V				–1.6	mA
I_{CCH}	High-level supply current	V_{CC} = MAX			29	41	mA
I_{CCL}	Low-level supply current	V_{CC} = MAX			21	30	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		6	10	ns
t_{PHL}					20	30	
t_{PLH}	A	Y	R_L = 150 Ω, C_L = 50 pF			15	ns
t_{PHL}						26	

6.7 Typical Characteristics

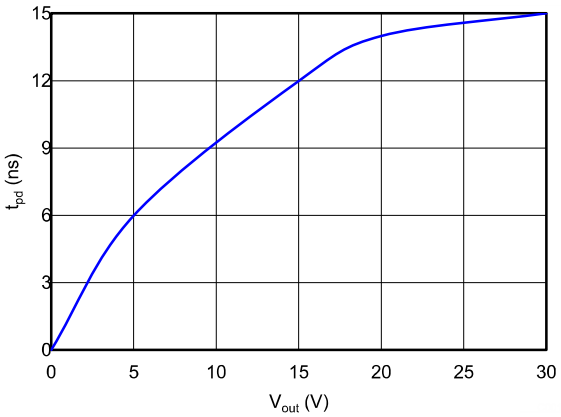
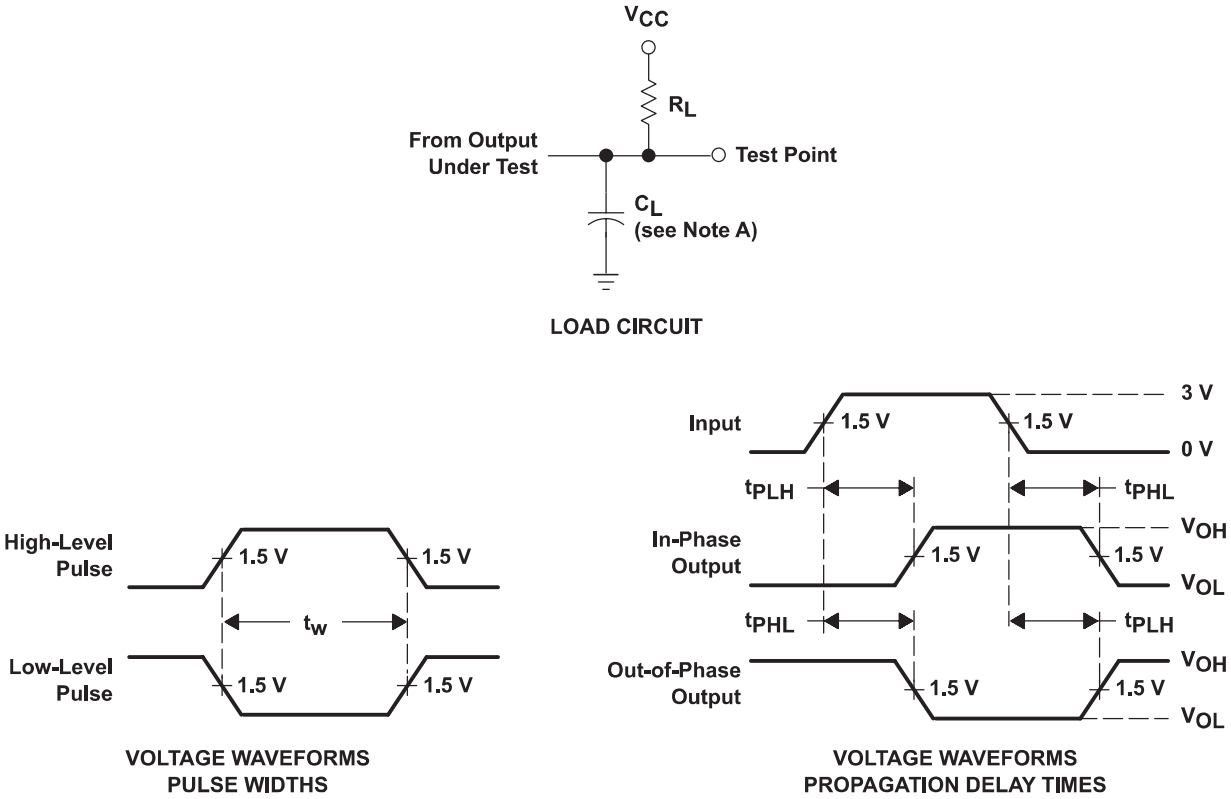


Figure 1. Time Low to High vs V_{OUT}

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 7 ns, t_f ≤ 7 ns.

D. The outputs are measured one at a time, with one input transition per measurement.

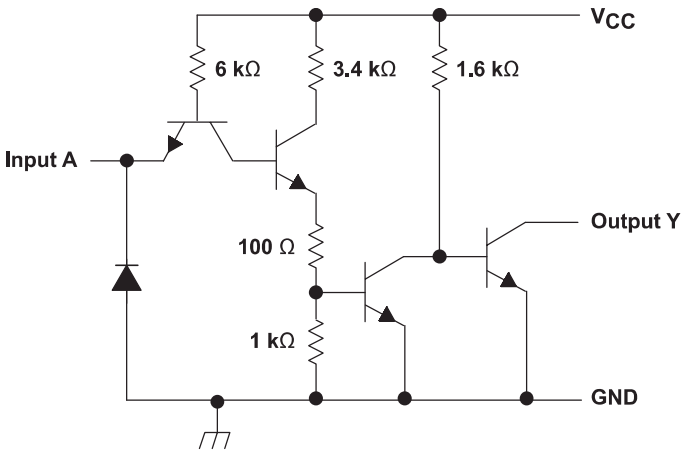
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74x7 is a high sink current capable open-collector buffer. This device is high-voltage tolerant on the output of up to 30 V on the SNx407 model and 15 V on the SNx417 model. The SN74x7 is also useful for converting TTL voltage levels to MOS levels.

8.2 Functional Block Diagram



Resister values shown are nominal.

Figure 3. Schematic

8.3 Feature Description

The SNx407 and SNx417 devices are ideal for high voltage outputs. The SNx407 device has a maximum output voltage 30 V and the SNx417 device has a maximum output voltage 15 V.

The high sink current is up to 40 mA for the SN74x7.

8.4 Device Functional Modes

Table 1 lists the functions of the devices.

Table 1. Function Table

INPUT A	OUTPUT Y
H	High-Z
L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74x7 device is a high-drive, open-collector device that is used for multiple buffer-type functions. The device produces 30 mA of drive current. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The outputs are high voltage tolerant up to 30 V for the SNx407.

9.2 Typical Application

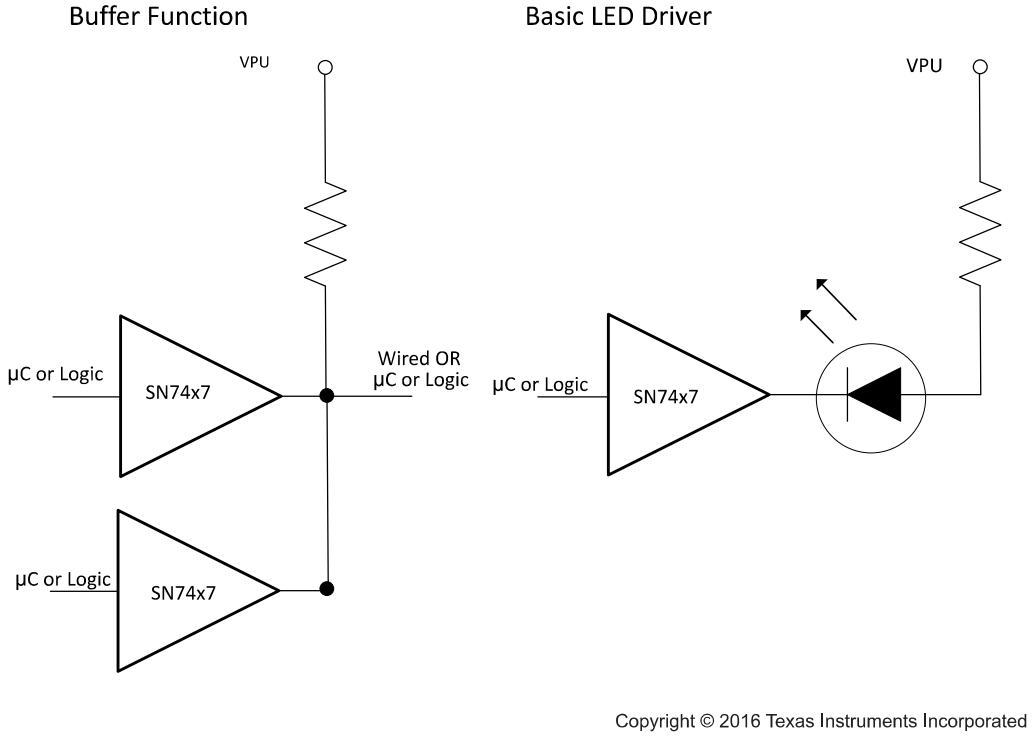


Figure 4. Typical Application Diagram

9.2.1 Design Requirements

Avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See t_{PHL} and t_{PLH} in *Switching Characteristics*.
   - Specified high and low levels: See V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommend Output Conditions
   - Load currents must not exceed 30 mA.
   - Outputs must not be pulled above 30 V for the SNx407 device.

Typical Application (continued)

9.2.3 Application Curve

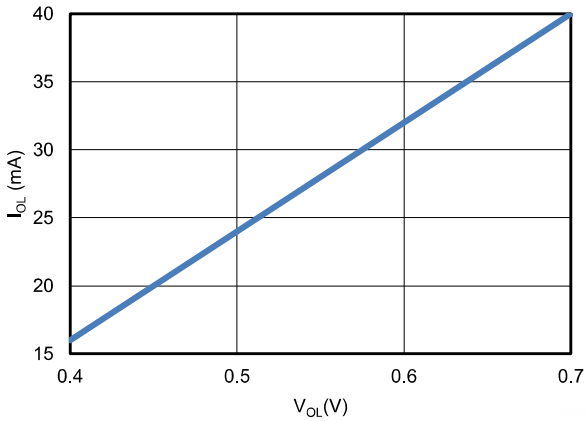


Figure 5. V_{OL} vs I_{OL}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating (see *Recommended Operating Conditions*).

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. TI recommends 0.1 µF for devices with a single supply. If there are multiple V_{CC} pins, then TI recommends 0.01 µF or 0.022 µF for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

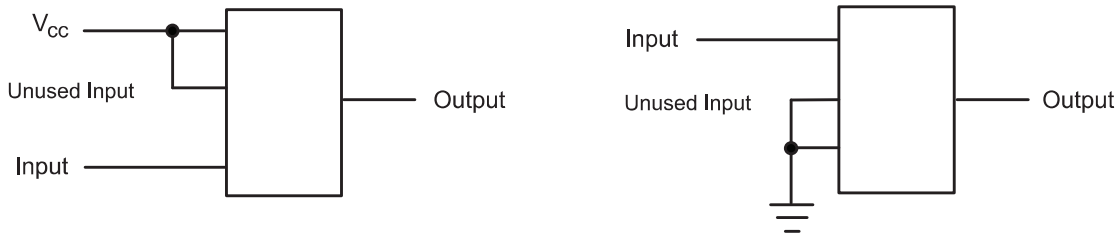


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN5407	Click here	Click here	Click here	Click here	Click here
SN5417	Click here	Click here	Click here	Click here	Click here
SN7407	Click here	Click here	Click here	Click here	Click here
SN7417	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me*to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
Blu-ray Disc is a registered trademark of Blue-ray Disc Association.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.