

CMOS 4-Stage Parallel In/Parallel Out Shift Register

with J-K Serial Inputs and True/Complement Outputs

High-Voltage Types (20-Volt Rating)

■ CD4035B is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J-K input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J-K inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})		
Voltages referenced to V _{SS} Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P _D):		
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- JK inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Buffered inputs and outputs
- High speed - 12 MHz (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications:

- Counters, Registers
- Arithmetic-unit registers
- Shift-left - shift right registers
- Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion

FIRST STAGE TRUTH TABLE

CL	t _{n-1} (INPUTS)				Q _{n-1}	t _n (OUTPUTS)
	J	K	R	R		
	0	X	0	0	0	0
	1	X	0	0	0	1
	X	0	0	0	1	0
	1	0	0	Q _{n-1}	Q _{n-1}	TOGGLE MODE
	X	1	0	1	1	
	X	X	0	Q _{n-1}	Q _{n-1}	
	X	X	1	X	0	

CD4035B Types

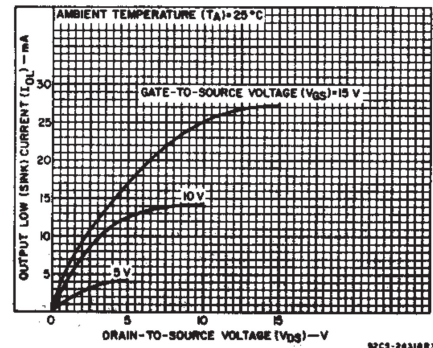
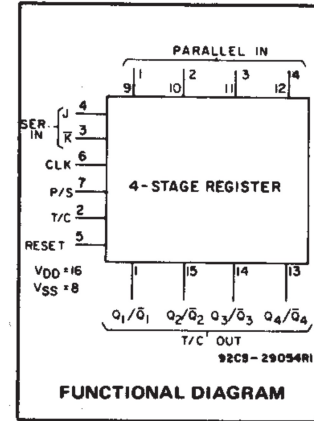


Fig. 1 - Typical output low (sink) current characteristics.

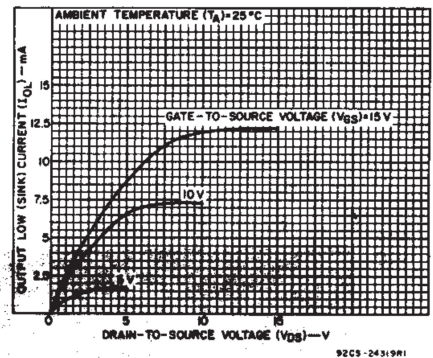


Fig. 2 - Minimum output low (sink) current characteristics.

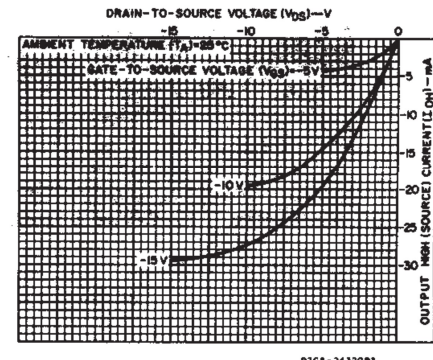


Fig. 3 - Typical output high (source) current characteristics.

CD4035B Types

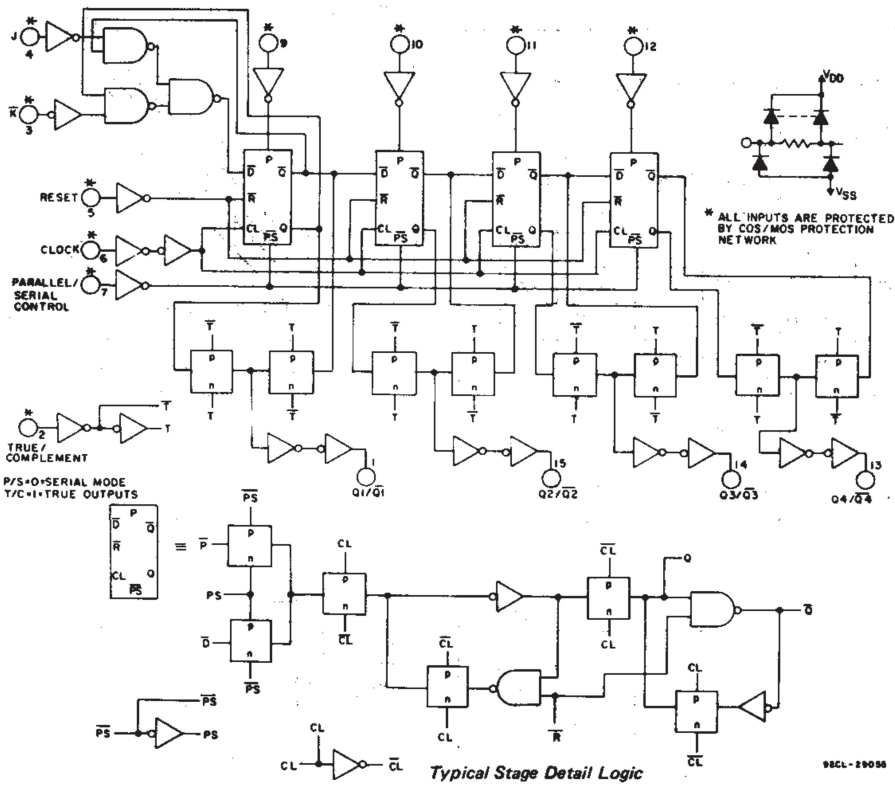


Fig. 4 - Logic diagram.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Data Setup Time, t_s : J/ \bar{K} Lines	5	220	—	ns
	10	80	—	
	15	60	—	
Parallel-In Lines	5	140	—	ns
	10	50	—	
	15	40	—	
Clock Pulse Width, t_W	5	200	—	ns
	10	90	—	
	15	60	—	
Clock Input Frequency, f_{CL}	5	—	2	MHz
	10	dc	6	
	15	—	8	
Clock Rise or Fall Time, t_{rCL} , t_{fCL} :	5	—	15	μs
	10	—	15	
	15	—	15	
Reset Pulse Width, t_W	5	250	—	ns
	10	110	—	
	15	80	—	

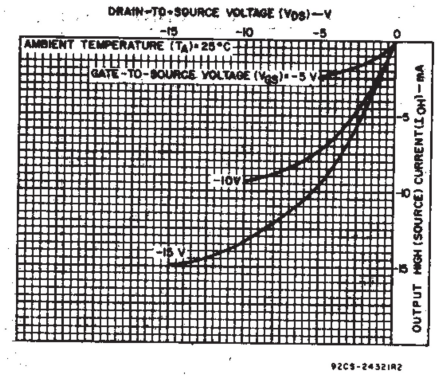


Fig. 5 - Minimum output high (source) current characteristics.

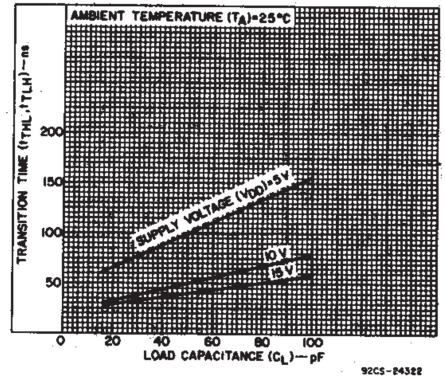


Fig. 6 - Typical transition time as a function of load capacitance.

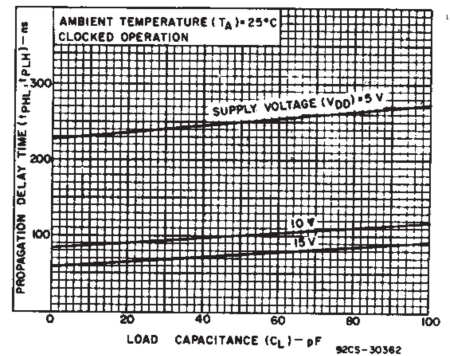


Fig. 7 - Typical propagation delay times as a function of load capacitance (Q output).

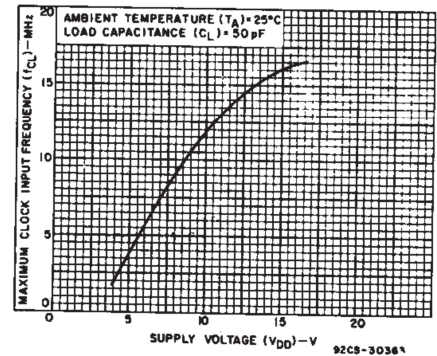


Fig. 8 - Typical maximum clock input frequency as a function of supply voltage.

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 COMMERCIAL CMOS
 HIGH VOLTAGE ICs

CD4035B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current, I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

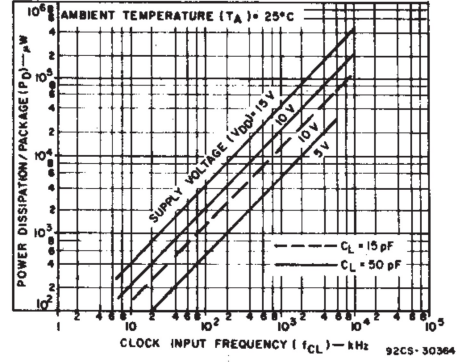


Fig. 9 - Typical dynamic power dissipation as a function of clock input frequency.

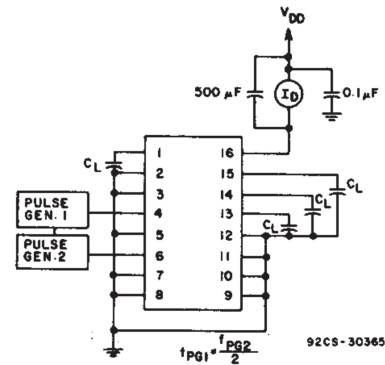


Fig. 10 - Dynamic power dissipation test circuit.

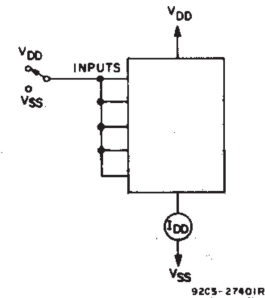


Fig. 11 - Quiescent-device current test circuit.

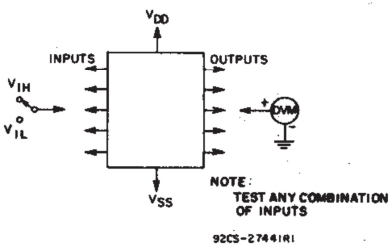


Fig. 12 - Input-voltage test circuit.

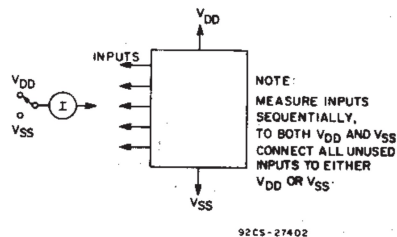


Fig. 13 - Input-current test circuit.

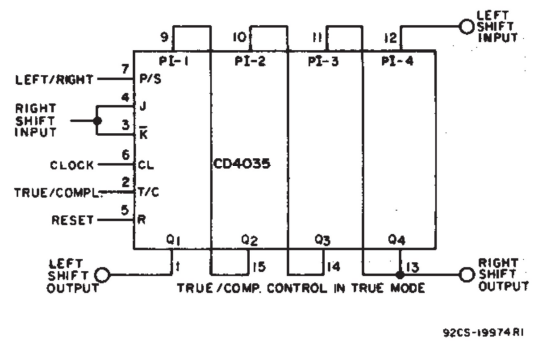
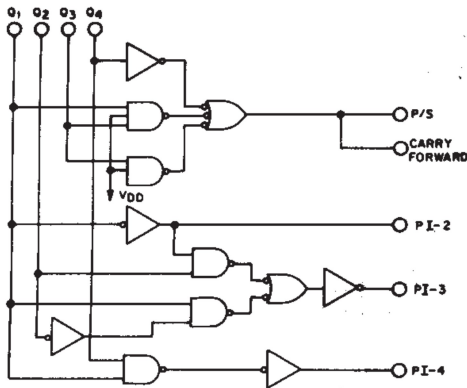


Fig. 14 - Shift left/shift right register.

CD4035B Types



Using Couleur's Technique (BIDECE)[▲], a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035B, with the correct conversion logic, can also be used as a BCD-to-binary converter.

[▲]The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313-316.

Fig. 15 - BIDECE logic.

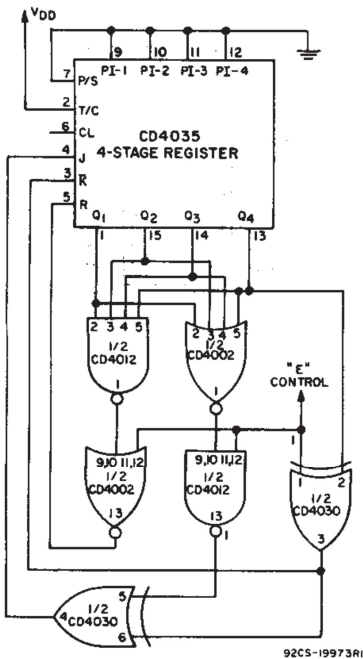


Fig. 16(a) - Double sequence generator.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS					
		V _{DD} (V)	Min.	Typ.		Max.				
CLOCKED OPERATION										
Propagation Delay Time: t_{PHL}, t_{PLH}		5	—	250	500	ns				
		10	—	100	200					
		15	—	75	150					
Transition Time: t_{THL}, t_{TLH}		5	—	100	200	ns				
		10	—	50	100					
		15	—	40	80					
Minimum Clock Pulse Width, t_{W}		5	—	100	200	ns				
		10	—	45	90					
		15	—	30	60					
Clock Rise or Fall Time, t_{rCL}, t_{fCL}^*		5, 10, 15	—	—	15	μs				
		5	—	110	220		ns			
		10	—	40	80					
Minimum Setup Time: J/K Lines		15	—	30	60	ns				
		5	—	70	140		ns			
		10	—	25	50					
Parallel-In-Lines		15	—	20	40	ns				
		5	2	4	—		MHz			
		10	6	12	—					
Maximum Clock Frequency, f_{CL}		15	8	16	—	MHz				
		Input Capacitance, C_{IN}		Any Input			—	5	7.5	pF
		RESET OPERATION								
Propagation Delay Time: t_{PHL}, t_{PLH}		5	—	230	460	ns				
		10	—	100	200					
		15	—	80	160					
Minimum Reset Pulse Width, t_{W}		5	—	125	250	ns				
		10	—	55	110					
		15	—	40	40					

*If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Control # E =	0				1			
	Q ₁	Q ₂	Q ₃	Q ₄	Q ₁	Q ₂	Q ₃	Q ₄
A	0	0	0	0	15	1	1	1
B	1	1	0	0	14	0	1	1
C	2	0	1	0	13	1	0	1
D	5	1	0	1	10	0	1	0
0	10	0	1	0	5	1	0	1
1	4	0	0	1	11	1	0	1
2	9	1	0	0	6	0	1	0
3	3	1	1	0	12	0	0	1
4	6	0	1	1	9	1	0	0
5	13	1	0	1	2	0	1	0
6	11	1	1	0	4	0	0	1
7	7	1	1	1	8	0	0	0
8	14	0	1	1	1	1	0	0
9	12	0	0	1	3	1	1	0
10	8	0	0	1	7	1	1	0

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Fig. 16(b) - State sequences.

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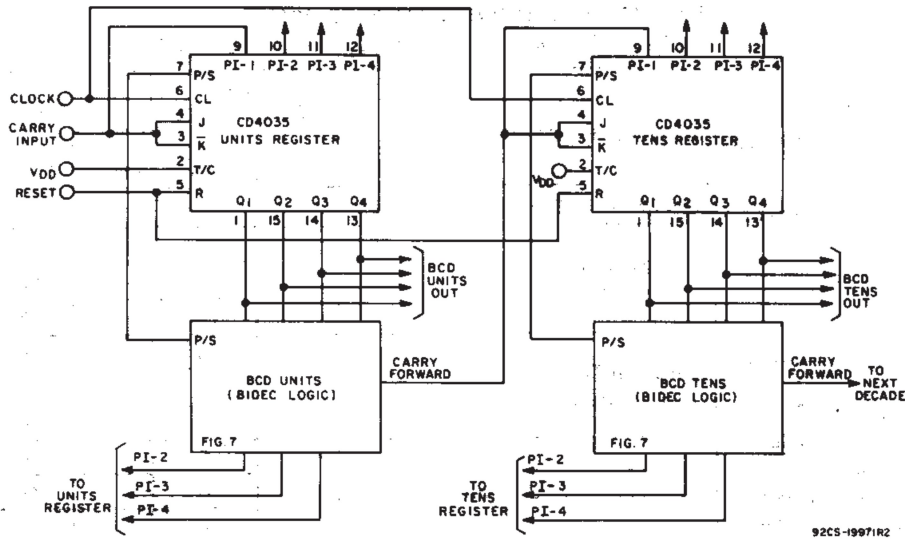
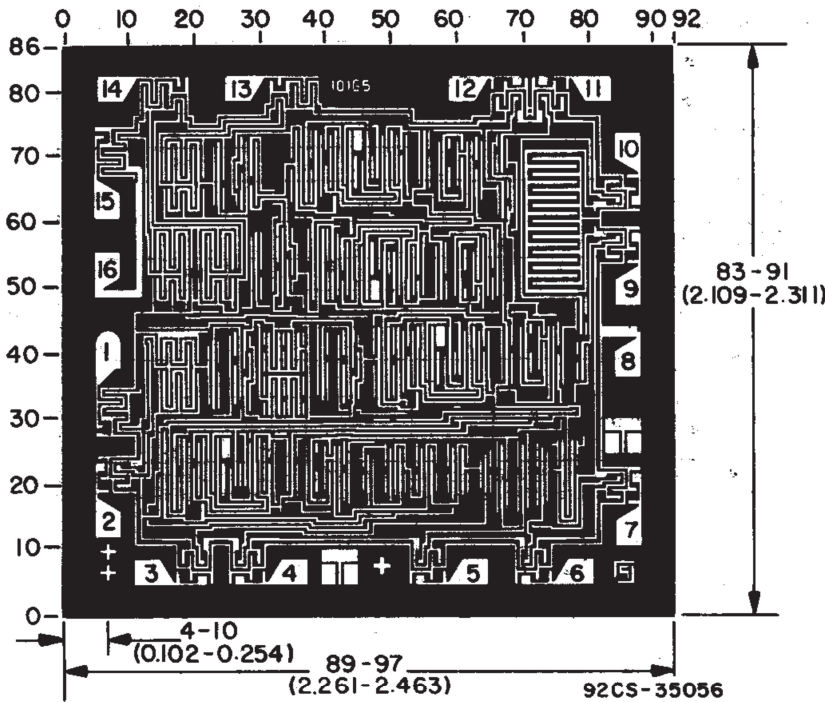
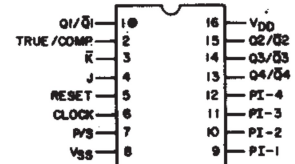


Fig. 17 - Binary-to-BCD converter.



TERMINAL DIAGRAM Top View



92CS-20745R1

Dimensions and pad layout for CD4035BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).