

# CD4014B, CD4021B Types

## CMOS 8-Stage Static Shift Registers

High-Voltage Types (20-Volt Rating)

**CD4014B:**

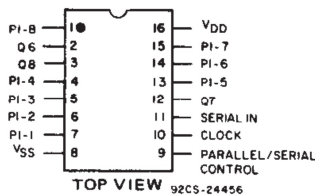
Synchronous Parallel or Serial Input/Serial Output

**CD4021B:**

Asynchronous Parallel Input or Synchronous Serial Input/Serial Output

■ CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

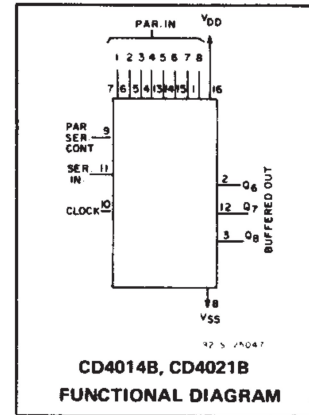
The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



TOP VIEW 92CS-24456  
**TERMINAL DIAGRAM**  
CD4014B, CD4021B

**Features:**

- Medium-speed operation . . . 12 MHz (typ.) clock rate at  $V_{DD}-V_{SS} = 10\text{ V}$
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at  $V_{DD} = 5\text{ V}$   
2 V at  $V_{DD} = 10\text{ V}$   
2.5 V at  $V_{DD} = 15\text{ V}$
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



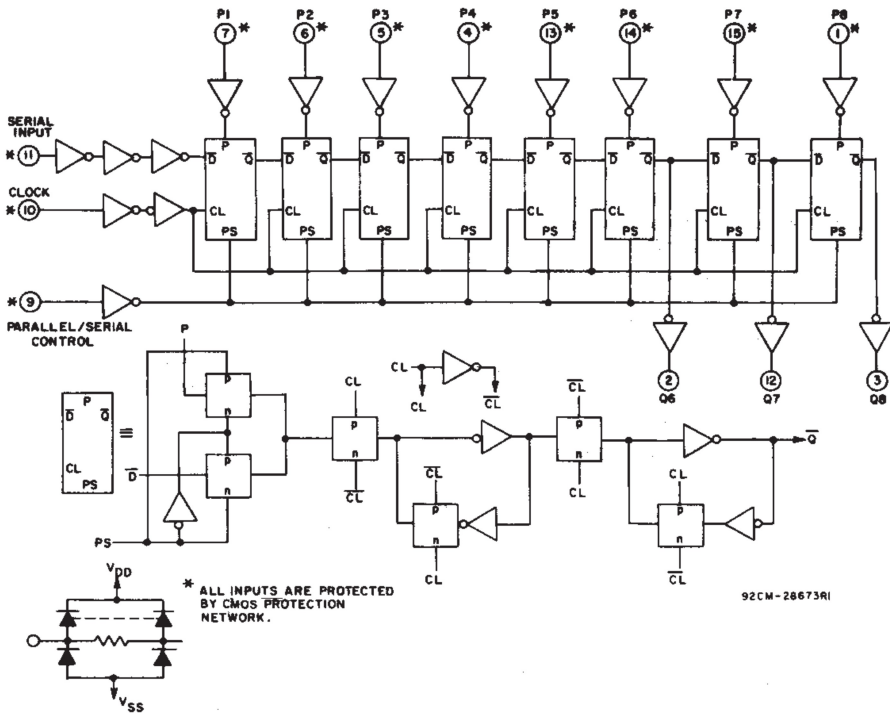
**Applications:**

- Parallel input/serial output data queuing
- Parallel to serial data conversion
- General-purpose register

**RECOMMENDED OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified**  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC   | $V_{DD}$ (V) | LIMITS |      | UNITS         |
|--|--------------|--------|------|---------------|
|  |              | Min.   | Max. |               |
| Supply-Voltage Range ( $T_A = \text{Full Package-Temperature Range}$ ) | —            | 3      | 18   | V             |
| Clock Pulse Width, $t_W$   | 5            | 180    | —    | ns            |
|  | 10           | 80     | —    |               |
|  | 15           | 50     | —    |               |
| Clock Frequency, $f_{CL}$  | 5            | —      | 3    | MHz           |
|  | 10           | —      | 6    |               |
|  | 15           | —      | 8.5  |               |
| Clock Rise and Fall Time, $t_rCL, t_fCL$                               | 5            | —      | 15   | $\mu\text{s}$ |
|  | 10           | —      | 15   |               |
|  | 15           | —      | 15   |               |
| Set-up Time, $t_s$ :   |              |        |      |               |
| Serial Input (ref. to CL)  | 5            | 120    | —    | ns            |
|  | 10           | 80     | —    |               |
|  | 15           | 60     | —    |               |
| Parallel Inputs CD4014B (ref. to CL)                                   | 5            | 80     | —    | ns            |
|  | 10           | 50     | —    |               |
|  | 15           | 40     | —    |               |
| Parallel Inputs CD4021B (ref. to P/S)                                  | 5            | 50     | —    | ns            |
|  | 10           | 30     | —    |               |
|  | 15           | 20     | —    |               |
| Parallel/Serial Control (ref. to CL)                                   | 5            | 180    | —    | ns            |
|  | 10           | 80     | —    |               |
|  | 15           | 60     | —    |               |
| Parallel/Serial Pulse Width, $t_W$ (CD4021B)                           | 5            | 160    | —    | ns            |
|  | 10           | 80     | —    |               |
|  | 15           | 50     | —    |               |
| Parallel/Serial Removal Time, $t_{REM}$ (CD4021B)                      | 5            | 280    | —    | ns            |
|  | 10           | 140    | —    |               |
|  | 15           | 100    | —    |               |

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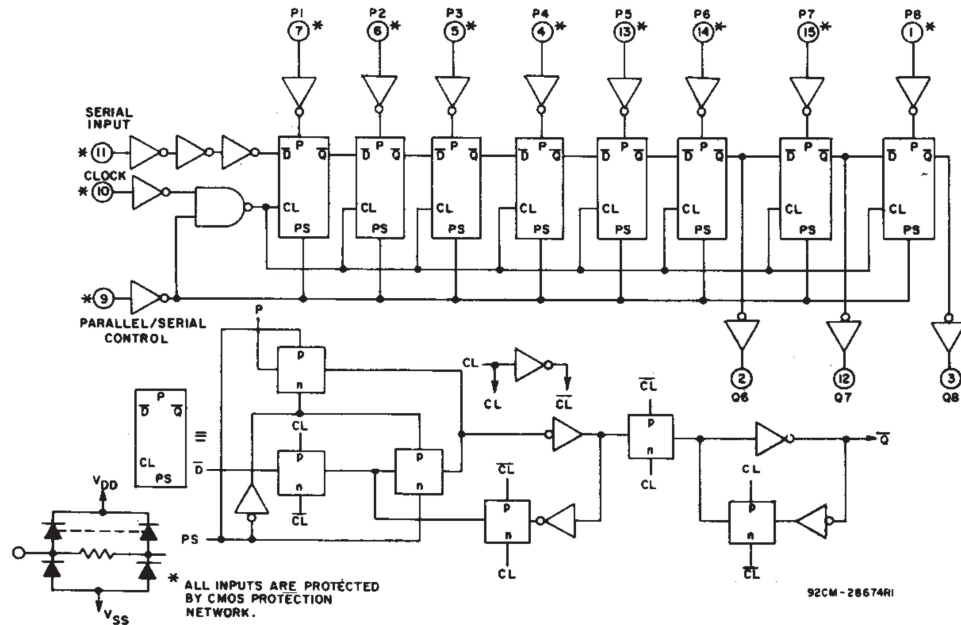


TRUTH TABLE – CD4014B

| CL | SER IN | PAR SER CONTROL | PI-1 | PI-n | Q1 (INTERNAL)  | Qn               |
|----|--------|-----------------|------|------|----------------|------------------|
| /  | X      | 1               | 0    | 0    | 0              | 0                |
| /  | X      | 1               | 1    | 0    | 1              | 0                |
| /  | X      | 1               | 0    | 1    | 0              | 1                |
| /  | X      | 1               | 1    | 1    | 1              | 1                |
| /  | 0      | 0               | X    | X    | 0              | Q <sub>n-1</sub> |
| /  | 1      | 0               | X    | X    | 1              | Q <sub>n-1</sub> |
| /  | X      | X               | X    | X    | Q <sub>1</sub> | Q <sub>n</sub>   |

X = DON'T CARE CASE  
NC = NO CHANGE

Fig. 1 – Logic diagram for CD4014B.



TRUTH TABLE – CD4021B

| CL | Serial Input | Parallel/Serial Control | PI-1 | PI-n | Q1 (Internal)  | Qn               |
|----|--------------|-------------------------|------|------|----------------|------------------|
| X  | X            | 1                       | 0    | 0    | 0              | 0                |
| X  | X            | 1                       | 0    | 1    | 0              | 1                |
| X  | X            | 1                       | 1    | 0    | 1              | 0                |
| X  | X            | 1                       | 1    | 1    | 1              | 1                |
| /  | 0            | 0                       | X    | X    | 0              | Q <sub>n-1</sub> |
| /  | 1            | 0                       | X    | X    | 1              | Q <sub>n-1</sub> |
| /  | X            | 0                       | X    | X    | Q <sub>1</sub> | Q <sub>n</sub>   |

X = DON'T CARE CASE

Fig. 2 – Logic diagram for CD4021B.

# CD4014B, CD4021B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |                                     |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )<br>Voltages referenced to V <sub>SS</sub> Terminal) | -0.5V to +20V                       |
| INPUT VOLTAGE RANGE, ALL INPUTS   | -0.5V to V <sub>DD</sub> +0.5V      |
| DC INPUT CURRENT, ANY ONE INPUT   | ±10mA                               |
| POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):  |                                     |
| For T <sub>A</sub> = -55°C to +100°C  | 500mW                               |
| For T <sub>A</sub> = +100°C to +125°C   | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR  |                                     |
| FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)                         | 100mW                               |
| OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )   | -55°C to +125°C                     |
| STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )   | -65°C to +150°C                     |
| LEAD TEMPERATURE (DURING SOLDERING):  |                                     |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max                              | +265°C                              |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|  |                    |                     |                     |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.     | -                  | 0.5                 | 5                   | 5                                     | 5     | 150   | 150   | -     | 0.04              | 5    | μA    |
|  | -                  | 0.10                | 10                  | 10                                    | 10    | 300   | 300   | -     | 0.04              | 10   |       |
|  | -                  | 0.15                | 15                  | 20                                    | 20    | 600   | 600   | -     | 0.04              | 20   |       |
|  | -                  | 0.20                | 20                  | 100                                   | 100   | 3000  | 3000  | -     | 0.08              | 100  |       |
| Output Low (Sink) Current, I <sub>OL</sub> Min.    | 0.4                | 0.5                 | 5                   | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | -    | mA    |
|  | 0.5                | 0.10                | 10                  | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | -    |       |
|  | 1.5                | 0.15                | 15                  | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | -    |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4.6                | 0.5                 | 5                   | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | -    | mA    |
|  | 2.5                | 0.5                 | 5                   | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | -    |       |
|  | 9.5                | 0.10                | 10                  | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | -    |       |
|  | 13.5               | 0.15                | 15                  | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | -    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.    | -                  | 0.5                 | 5                   | 0.05                                  |       |       |       | -     | 0                 | 0.05 | V     |
|  | -                  | 0.10                | 10                  | 0.05                                  |       |       |       | -     | 0                 | 0.05 |       |
|  | -                  | 0.15                | 15                  | 0.05                                  |       |       |       | -     | 0                 | 0.05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.   | -                  | 0.5                 | 5                   | 4.95                                  |       |       |       | 4.95  | 5                 | -    | V     |
|  | -                  | 0.10                | 10                  | 9.95                                  |       |       |       | 9.95  | 10                | -    |       |
|  | -                  | 0.15                | 15                  | 14.95                                 |       |       |       | 14.95 | 15                | -    |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 0.5, 4.5           | -                   | 5                   | 1.5                                   |       |       |       | -     | -                 | 1.5  | V     |
|  | 1.9                | -                   | 10                  | 3                                     |       |       |       | -     | -                 | 3    |       |
|  | 1.5, 13.5          | -                   | 15                  | 4                                     |       |       |       | -     | -                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0.5, 4.5           | -                   | 5                   | 3.5                                   |       |       |       | 3.5   | -                 | -    | V     |
|  | 1.9                | -                   | 10                  | 7                                     |       |       |       | 7     | -                 | -    |       |
|  | 1.5, 13.5          | -                   | 15                  | 11                                    |       |       |       | 11    | -                 | -    |       |
| Input Current I <sub>IN</sub> Max.                 | -                  | 0.18                | 18                  | ±0.1                                  | ±0.1  | ±1    | ±1    | -     | ±10 <sup>-5</sup> | ±0.1 | μA    |

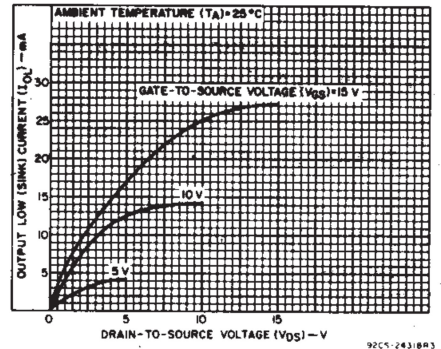


Fig. 3 - Typical output low (sink) current characteristics.

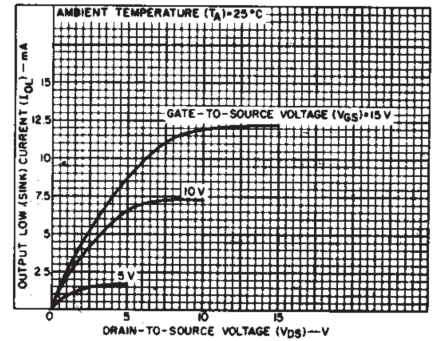


Fig. 4 - Minimum output low (sink) current characteristics.

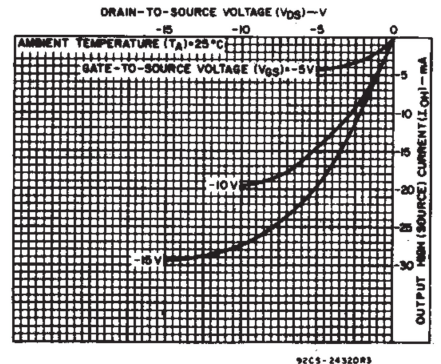


Fig. 5 - Typical output high (source) current characteristics.

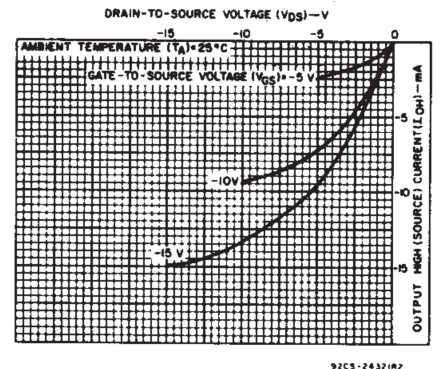


Fig. 6 - Minimum output high (source) current characteristics.

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## CD4014B, CD4021B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A=25^\circ\text{C}$ , Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$ ,  $R_L=200\text{ K}\Omega$

| CHARACTERISTIC   | TEST CONDITIONS | LIMITS              |      |      | UNITS         |
|--|-----------------|---------------------|------|------|---------------|
|  |                 | V <sub>DD</sub> (V) | Min. | Typ. |               |
| Propagation Delay Time, $t_{PLH}, t_{PHL}$                                       | 5               | —                   | 160  | 320  | ns            |
|  | 10              | —                   | 80   | 160  |               |
|  | 15              | —                   | 60   | 120  |               |
| Transition Time, $t_{THL}, t_{TLH}$  | 5               | —                   | 100  | 200  | ns            |
|  | 10              | —                   | 50   | 100  |               |
|  | 15              | —                   | 40   | 80   |               |
| Maximum Clock Input Frequency, $f_{CL}$  | 5               | 3                   | 6    | —    | MHz           |
|  | 10              | 6                   | 12   | —    |               |
|  | 15              | 8.5                 | 17   | —    |               |
| Minimum Clock Pulse Width, $t_{WP}$  | 5               | —                   | 90   | 180  | ns            |
|  | 10              | —                   | 40   | 80   |               |
|  | 15              | —                   | 25   | 50   |               |
| Clock Rise and Fall Time, $t_{r,CL}, t_{f,CL}^*$                                 | 5               | —                   | —    | 15   | $\mu\text{s}$ |
|  | 10              | —                   | —    | 15   |               |
|  | 15              | —                   | —    | 15   |               |
| Minimum Set-up Time, $t_s$ :<br>Serial Input<br>(ref. to CL)                     | 5               | —                   | 60   | 120  | ns            |
|  | 10              | —                   | 40   | 80   |               |
|  | 15              | —                   | 30   | 60   |               |
| Parallel Inputs<br>CD4014B<br>(ref. to CL)                                       | 5               | —                   | 40   | 80   | ns            |
|  | 10              | —                   | 25   | 50   |               |
|  | 15              | —                   | 20   | 40   |               |
| Parallel Inputs<br>CD4021B<br>(ref. to P/S)                                      | 5               | —                   | 25   | 50   | ns            |
|  | 10              | —                   | 15   | 30   |               |
|  | 15              | —                   | 10   | 20   |               |
| Parallel/Serial Control<br>CD4014B<br>(ref. to CL)                               | 5               | —                   | 90   | 180  | ns            |
|  | 10              | —                   | 40   | 80   |               |
|  | 15              | —                   | 30   | 60   |               |
| Minimum Hold Time, $t_H$ :<br>Serial In, Parallel In,<br>Parallel/Serial Control | 5               | —                   | —    | 0    | ns            |
|  | 10              | —                   | —    | 0    |               |
|  | 15              | —                   | —    | 0    |               |
| Minimum P/S Pulse Width,<br>$t_{WH}$<br>(CD4021B)                                | 5               | —                   | 80   | 160  | ns            |
|  | 10              | —                   | 40   | 80   |               |
|  | 15              | —                   | 25   | 50   |               |
| Minimum P/S Removal Time,<br>$t_{REM}$<br>CD4021B (ref. to CL)                   | 5               | —                   | 140  | 280  | ns            |
|  | 10              | —                   | 70   | 140  |               |
|  | 15              | —                   | 50   | 100  |               |
| Average Input Capacitance, $C_I$   | Any Input       | —                   | 5    | 7.5  | pF            |

\* If more than one unit is cascaded  $t_{r,CL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

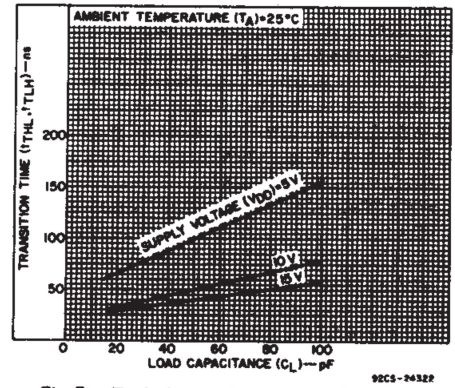


Fig. 7 — Typical transition time as a function of load capacitance.

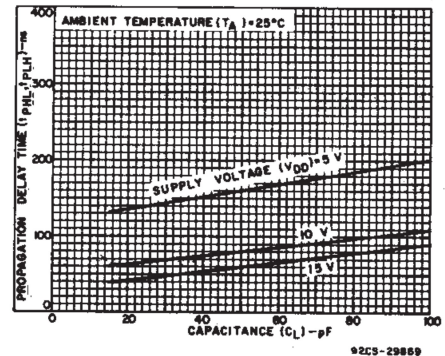


Fig. 8 — Typical propagation delay time as a function of load capacitance.

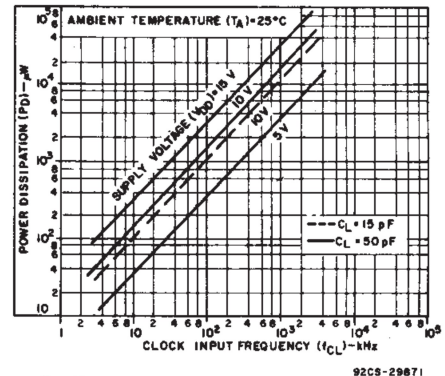


Fig. 9 — Typical dynamic power dissipation as a function of clock input frequency.

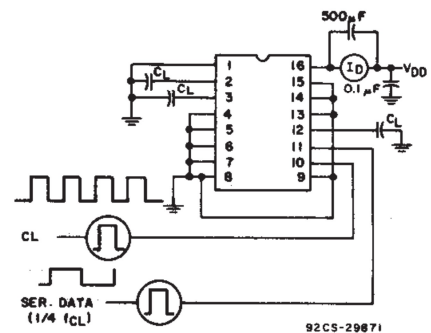


Fig. 10 — Dynamic power dissipation test circuit.

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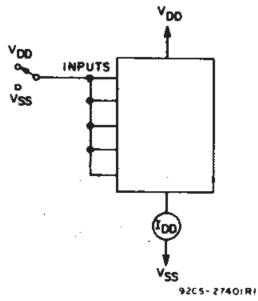


Fig. 11 - Quiescent device current test circuit.

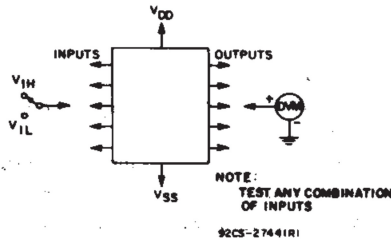


Fig. 12 - Input voltage test circuit.

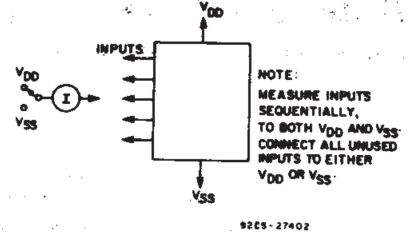
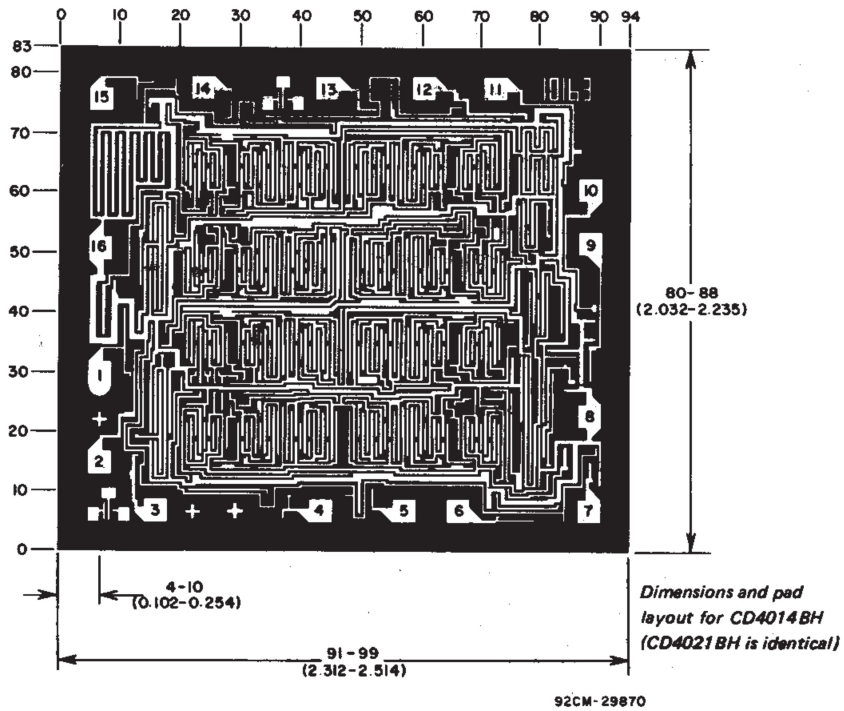


Fig. 13 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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