4-to-16 line decoder/demultiplexer 74HC154; 74HCT154

FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one 16 mutually exclusive outputs
- Complies with JEDEC standard no. 8-1 B
- ESD protection:
  HBM EIA/JESD22-A114-B exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74HC154; 74HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC154; 74HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs. The two-input enable gate can be used to strobe the decoder to eliminate the normal decoding “glitches” on the outputs, or can be used for the expansion of the decoder.

The enable gate has two ANDed inputs which must be LOW to enable the outputs.

The 74HC154; 74HCT154 can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable input is LOW, the addressed output will follow the state of the applied data.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC154	74HCT154	
t_{PHL}/t_{PLH}	propagation delay An, $\overline{En}$ to $\overline{Yn}$	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	11	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	60	60	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For 74HC154 the condition is V_I = GND to V_{CC}
   For 74HCT154 the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT						OUTPUT															
$\overline{E0}$	$\overline{E1}$	A0	A1	A2	A3	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y2}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don’t care.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74HC154N	–40 °C to +125 °C	24	DIP24	plastic	SOT101-1
74HCT154N	–40 °C to +125 °C	24	DIP24	plastic	SOT101-1
74HC154D	–40 °C to +125 °C	24	SO24	plastic	SOT137-1
74HCT154D	–40 °C to +125 °C	24	SO24	plastic	SOT137-1
74HC154DB	–40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74HCT154DB	–40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74HC154PW	–40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1
74HCT154PW	–40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1
74HC154BQ	–40 °C to +125 °C	24	DHVQFN24	plastic	SOT815-1
74HCT154BQ	–40 °C to +125 °C	24	DHVQFN24	plastic	SOT815-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{Y0}$	data output (active LOW)
2	$\overline{Y1}$	data output (active LOW)
3	$\overline{Y2}$	data output (active LOW)
4	$\overline{Y3}$	data output (active LOW)
5	$\overline{Y4}$	data output (active LOW)
6	$\overline{Y5}$	data output (active LOW)
7	$\overline{Y6}$	data output (active LOW)
8	$\overline{Y7}$	data output (active LOW)
9	$\overline{Y8}$	data output (active LOW)
10	$\overline{Y9}$	data output (active LOW)
11	$\overline{Y10}$	data output (active LOW)
12	GND	ground (0 V)
13	$\overline{Y11}$	data output (active LOW)
14	$\overline{Y12}$	data output (active LOW)
15	$\overline{Y13}$	data output (active LOW)
16	$\overline{Y14}$	data output (active LOW)
17	$\overline{Y15}$	data output (active LOW)
18	$\overline{E0}$	enable input
19	$\overline{E1}$	enable input
20	A3	data input
21	A2	data input
22	A1	data input
23	A0	data input
24	V_{CC}	positive supply voltage

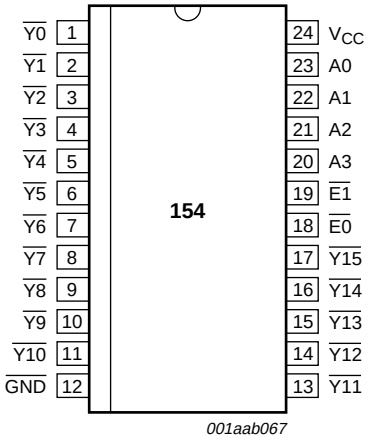
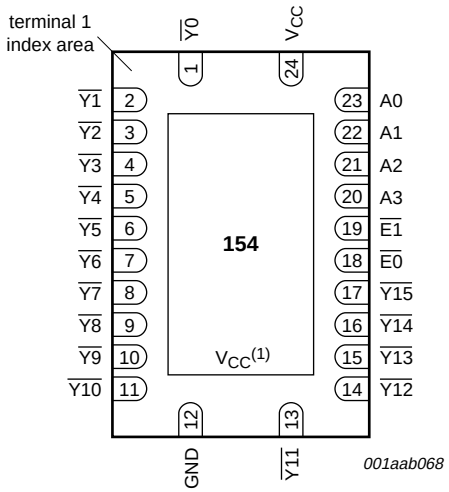


Fig.1 Pin configuration SO24, DIP24 and (T)SSOP24.



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN24.

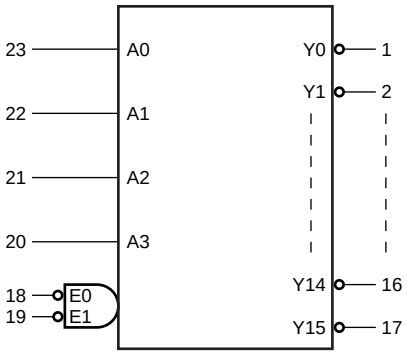


Fig.3 Logic symbol.

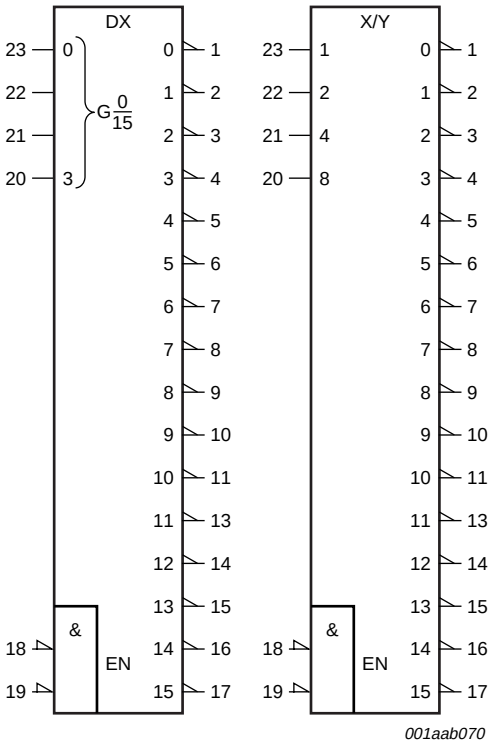


Fig.4 IEC logic symbol.