

# SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

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'290, 'LS290 . . . DECADE COUNTERS  
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

SN54290, SN54LS290, SN54293,  
SN54LS293 . . . J OR W PACKAGE  
SN74290, SN74293 . . . N PACKAGE  
SN74LS290, SN74LS293 . . . D OR N PACKAGE  
(TOP VIEW)

- GND and V<sub>CC</sub> on Corner Pins  
(Pins 7 and 14 Respectively)

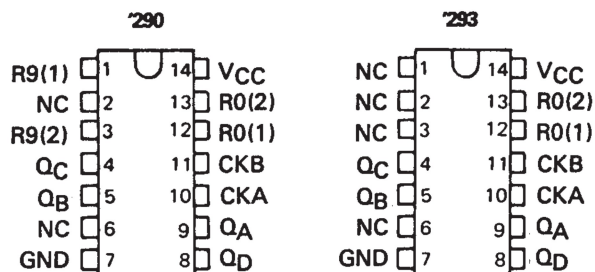
## description

The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

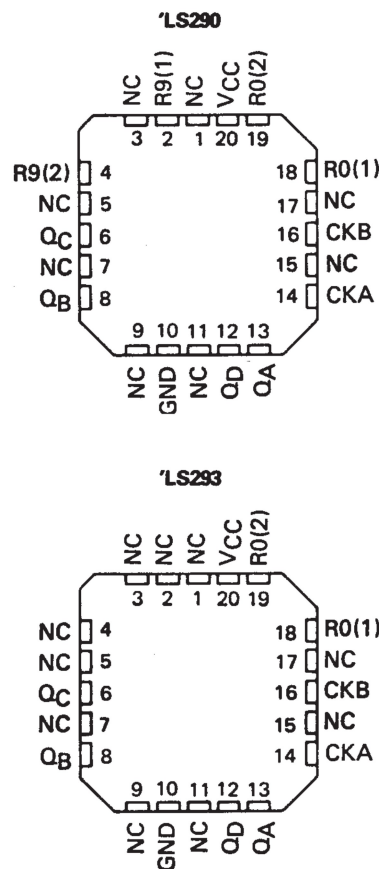
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q<sub>A</sub> output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q<sub>D</sub> output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q<sub>A</sub>.



SN54LS290, SN54LS293 . . . FK PACKAGE  
(TOP VIEW)

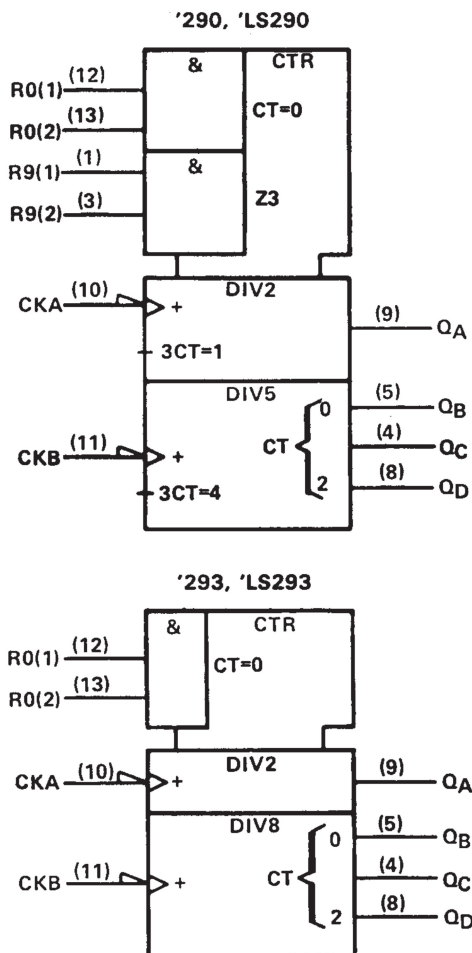


NC - No internal connection

SN54290, SN54293, SN54LS290, SN54LS293  
 SN74290, SN74293, SN74LS290, SN74LS293  
 DECADE AND 4-BIT BINARY COUNTERS

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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

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'290, 'LS290  
BCD COUNT SEQUENCE  
(See Note A)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'290, 'LS290  
BI-QUINARY (5-2)  
(See Note B)

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'290, 'LS290  
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R <sub>0</sub> (1)	R <sub>0</sub> (2)	R <sub>9</sub> (1)	R <sub>9</sub> (2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'293, 'LS293  
COUNT SEQUENCE  
(See Note C)

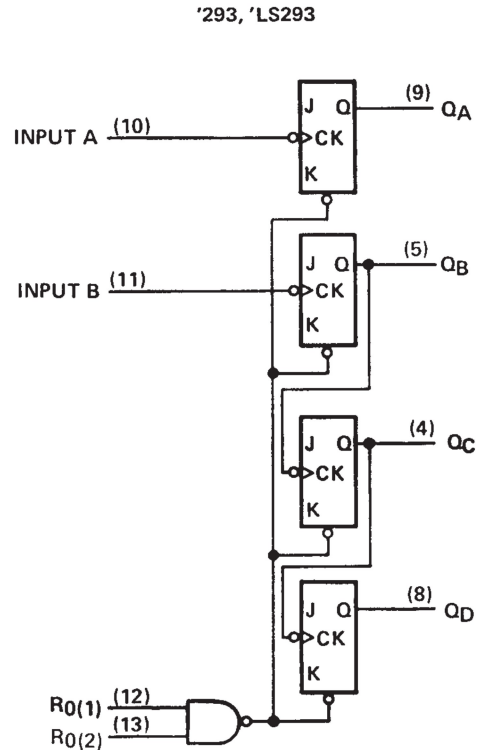
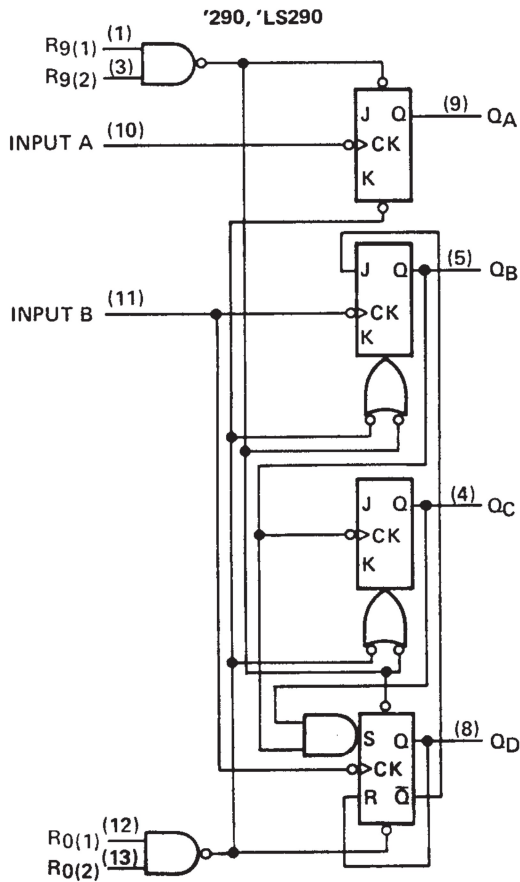
COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

- NOTES: A. Output Q<sub>A</sub> is connected to input B for BCD count.  
 B. Output Q<sub>D</sub> is connected to input A for bi-quinary count.  
 C. Output Q<sub>A</sub> is connected to input B.  
 D. H = high level, L = low level, X = irrelevant

'293, 'LS293  
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R <sub>0</sub> (1)	R <sub>0</sub> (2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

## logic diagrams (positive logic)



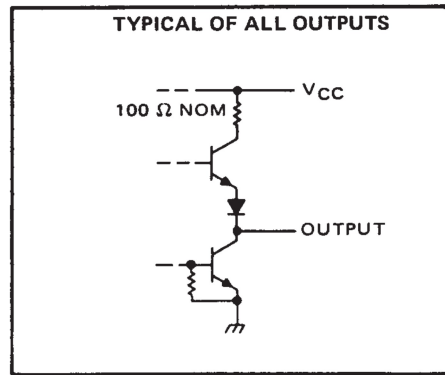
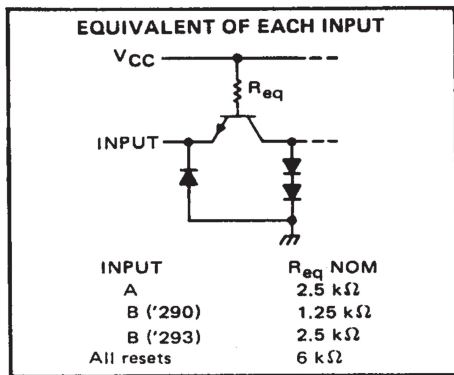
Pin numbers shown are for D, J, N, and W packages.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

# SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two  $R_0$  inputs, and for the '290 circuit, it also applies between the two  $R_9$  inputs.

## recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Count frequency, $f_{count}$	A input	0	32	0	32		MHz
	B input	0	16	0	16		
Pulse width, $t_w$	A input	15		15			ns
	B input	30		30			
	Reset inputs	15		15			
Reset inactive-state setup time, $t_{su}$	25			25			ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

SN54290, SN54293, SN54LS290, SN54LS293  
 SN74290, SN74293, SN74LS290, SN74LS293  
 DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'290			'293			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V <sub>IH</sub> High-level input voltage		2			2			V		
V <sub>IL</sub> Low-level input voltage				0.8			0.8	V		
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V		
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 μA	2.4	3.4		2.4	3.4		V		
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA¶		0.2	0.4		0.2	0.4	V		
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA		
I <sub>IH</sub> High-level input current	Any reset			40			40	μA		
	A input	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V							80	
	B input								120	80
I <sub>IL</sub> Low-level input current	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V						-1.6	mA	
	A input							-3.2		-3.2
	B input							-4.8		-3.2
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX	SN54'	-20	-57	-20	-57	mA			
		SN74'	-18	-57	-18	-57				
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 3		29	42		26	39	mA		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

¶ Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = 16 mA plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	A	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 4	32	42		32	42	MHz	
	B	Q <sub>B</sub>		16			16			
t <sub>PLH</sub>	A	Q <sub>A</sub>		10	16		10	16	ns	
t <sub>PHL</sub>				12	18		12	18		
t <sub>PLH</sub>	A	Q <sub>D</sub>		32	48		46	70	ns	
t <sub>PHL</sub>				34	50		46	70		
t <sub>PLH</sub>	B	Q <sub>B</sub>		10	16		10	16	ns	
t <sub>PHL</sub>				14	21		14	21		
t <sub>PLH</sub>	B	Q <sub>C</sub>		21	32		21	32	ns	
t <sub>PHL</sub>				23	35		23	35		
t <sub>PLH</sub>	B	Q <sub>D</sub>		21	32		34	51	ns	
t <sub>PHL</sub>				23	35		34	51		
t <sub>PHL</sub>	Set-to-0	Any		26	40		26	40	ns	
t <sub>PLH</sub>	Set-to-9	Q <sub>A</sub> , Q <sub>D</sub>		20	30				ns	
t <sub>PHL</sub>		Q <sub>B</sub> , Q <sub>C</sub>	26	40						

# f<sub>max</sub> = maximum count frequency

t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

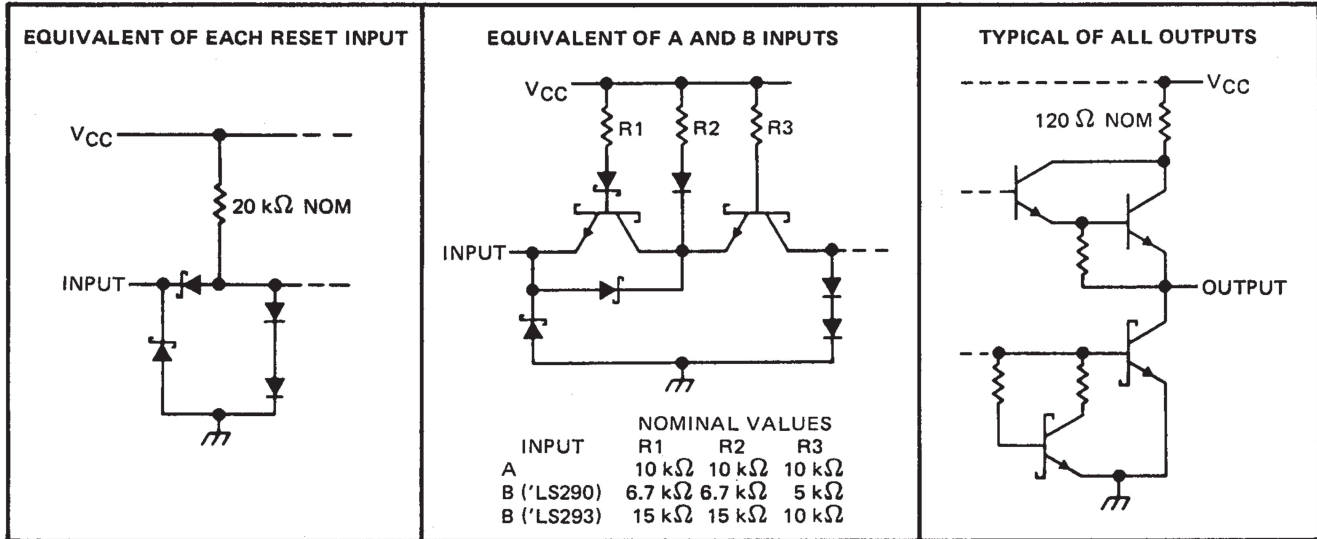
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



# SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 5)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293	-55°C to 125°C
SN74LS290, SN74LS293	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	μA
Low-level output current, $I_{OL}$			4			8	mA
Count frequency, $f_{count}$	A input	0	32	0	32		MHz
	B input	0	16	0	16		
Pulse width, $t_w$	A input	15		15			ns
	B input	30		30			
	Reset inputs	30		30			
Reset inactive-state setup time, $t_{SU}$		25			25		ns
Operating free-air temperature, $T_A$		-55	125		0	70	°C

SN54290, SN54293, SN54LS290, SN54LS293  
SN74290, SN74293, SN74LS290, SN74LS293  
DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IH</sub>	High-level input voltage		2			2			V	
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 4 mA¶			0.25 0.4			V	
			I <sub>OL</sub> = 8 mA¶			0.35 0.5				
I <sub>I</sub>	Input current at maximum input voltage	Any reset		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1 0.1			mA	
		A input				0.2 0.2				
		B of 'LS290		V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		0.4 0.4				
		B of 'LS293				0.2 0.2				
I <sub>IH</sub>	High-level input current	Any reset		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20 20			μA	
		A input				40 40				
		B of 'LS290				80 80				
		B of 'LS293				40 40				
I <sub>IL</sub>	Low-level input current	Any reset		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4 -0.4			mA	
		A input				-2.4 -2.4				
		B of 'LS290				-3.2 -3.2				
		B of 'LS293				-1.6 -1.6				
I <sub>OS</sub>	Short-circuit output current §	V <sub>CC</sub> = MAX		-20	-100	-20	-100		mA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 3		'LS290			9 15			mA
				'LS293			9 15			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290			'LS293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	A	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 4	32	42		32	42		MHz
	B	Q <sub>B</sub>		16			16			
t <sub>PLH</sub>	A	Q <sub>A</sub>		10	16		10	16		ns
t <sub>PHL</sub>				12	18		12	18		
t <sub>PLH</sub>	A	Q <sub>D</sub>		32	48		46	70		ns
t <sub>PHL</sub>				34	50		46	70		
t <sub>PLH</sub>	B	Q <sub>B</sub>		10	16		10	16		ns
t <sub>PHL</sub>				14	21		14	21		
t <sub>PLH</sub>	B	Q <sub>C</sub>		21	32		21	32		ns
t <sub>PHL</sub>				23	35		23	35		
t <sub>PLH</sub>	B	Q <sub>D</sub>		21	32		34	51		ns
t <sub>PHL</sub>				23	35		34	51		
t <sub>PHL</sub>	Set-to-0	Any		26	40		26	40		ns
t <sub>PLH</sub>	Set-to-9	Q <sub>A</sub> , Q <sub>D</sub>		20	30					ns
t <sub>PHL</sub>		Q <sub>B</sub> , Q <sub>C</sub>		26	40					

# f<sub>max</sub> = maximum count frequency

t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

