- **Can Be Used as a 4-Bit Digital Comparator**
- **Input Clamping Diodes Simplify System Design**
- **Fully Compatible with Most TTL Circuits**

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

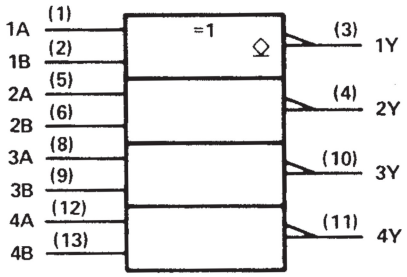
H = high level, L = low level

## description

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

## logic symbol (each gate)


## logic symbol†

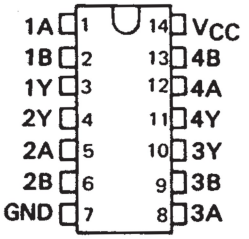



positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

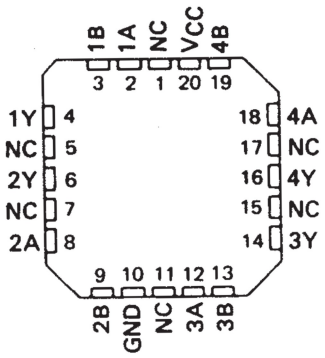
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

**SN54LS266 . . . J OR W PACKAGE**
**SN74LS266 . . . D OR N PACKAGE**
**(TOP VIEW)**

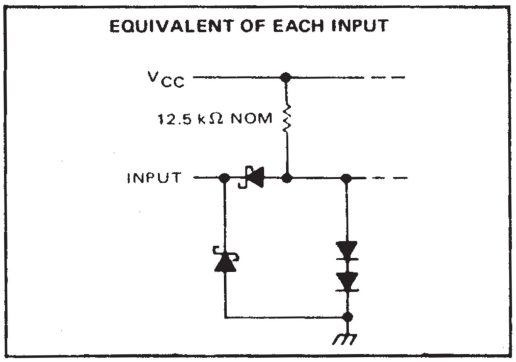


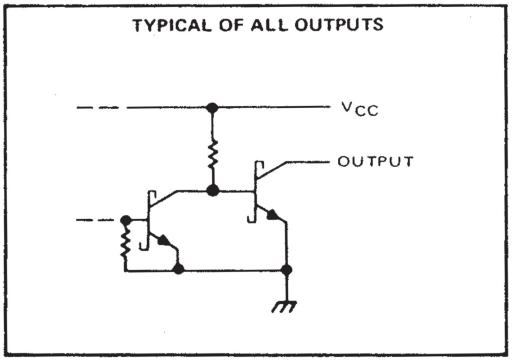

**SN54LS266 . . . FK PACKAGE**
**(TOP VIEW)**




NC - No internal connection

## schematic of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS266 . . . . . –55°C to 125°C
SN74LS266 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | SN54LS266 | | | SN74LS266 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, $V_{OH}$ | | | 5.5 | | | 5.5 | V |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS266 | | | SN74LS266 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = –18 mA | | | –1.5 | | | –1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $V_{OH}$ = 5.5 V | | | 100 | | | 100 | µA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.2 | | | 0.2 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 40 | | | 40 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | –0.8 | | | –0.8 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | See Note 2 | | 8 | 13 | | 8 | 13 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: $I_{CC}$ is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER§ | FROM (INPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A or B | Other input low | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 18 | 30 | ns |
| $t_{PHL}$ | | | | | 18 | 30 | |
| $t_{PLH}$ | A or B | Other input high | | | 18 | 30 | ns |
| $t_{PHL}$ | | | | | 18 | 30 | |

§$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.