

## LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

 Check for Samples: [LF147](#), [LF347-N](#)

### FEATURES

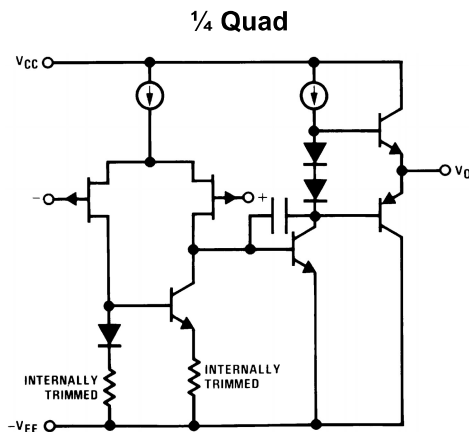
- **Internally Trimmed Offset Voltage: 5 mV max**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 7.2 mA**
- **High Input Impedance: 10<sup>12</sup>Ω**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 μs**

### DESCRIPTION

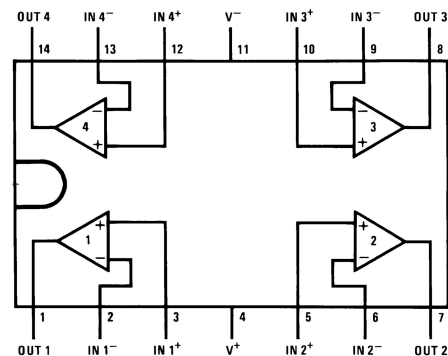
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage ( BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

### Simplified Schematic



### Connection Diagram



LF147 available as per JM38510/11906.

**Figure 1. 14-Pin PDIP / CDIP / SOIC  
Top View  
See Package Number J0014A, D0014A or  
NFF0014A**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BI-FET II is a trademark of dcl\_owner.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Absolute Maximum Ratings** <sup>(1)(2)</sup>

		LF147	LF347B/LF347
Supply Voltage		±22V	±18V
Differential Input Voltage		±38V	±30V
Input Voltage Range <sup>(3)</sup>		±19V	±15V
Output Short Circuit Duration <sup>(4)</sup>		Continuous	Continuous
Power Dissipation <sup>(5) (6)</sup>		900 mW	1000 mW
T <sub>j</sub> max		150°C	150°C
θ <sub>JA</sub>	CDIP (J) Package		70°C/W
	PDIP (NFF) Package		75°C/W
	SOIC Narrow (D)		100°C/W
	SOIC Wide (D)		85°C/W
Operating Temperature Range		See <sup>(7)</sup>	See <sup>(7)</sup>
Storage Temperature Range		-65°C ≤ T <sub>A</sub> ≤ 150°C	
Lead Temperature (Soldering, 10 sec.)		260°C	260°C
Soldering Information	PDIP / CDIP	Soldering (10 seconds)	
	SOIC Package	Vapor Phase (60 seconds)	
		Infrared (15 seconds)	
ESD Tolerance <sup>(8)</sup>			900V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- (4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (5) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ<sub>JA</sub>.
- (6) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside ensured limits.
- (7) The LF147 is available in the military temperature range -55°C ≤ T<sub>A</sub> ≤ 125°C, while the LF347B and the LF347 are available in the commercial temperature range 0°C ≤ T<sub>A</sub> ≤ 70°C. Junction temperature can rise to T<sub>j</sub> max = 150°C.
- (8) Human body model, 1.5 kΩ in series with 100 pF.

**DC Electrical Characteristics** <sup>(1)(2)</sup>

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>OS</sub>	Input Offset Voltage	R <sub>S</sub> =10 kΩ, T <sub>A</sub> =25°C Over Temperature		1	5		3	5		5	10	mV
					8		7			13		mV
ΔV <sub>OS</sub> /ΔT	Average TC of Input Offset Voltage	R <sub>S</sub> =10 kΩ		10			10			10		μV/°C
I <sub>OS</sub>	Input Offset Current	T <sub>j</sub> =25°C, <sup>(2) (3)</sup> Over Temperature		25	100		25	100		25	100	pA
					25		4			4		nA
I <sub>B</sub>	Input Bias Current	T <sub>j</sub> =25°C, <sup>(2) (3)</sup> Over Temperature		50	200		50	200		50	200	pA
					50		8			8		nA
R <sub>IN</sub>	Input Resistance	T <sub>j</sub> =25°C		10 <sup>12</sup>			10 <sup>12</sup>			10 <sup>12</sup>		Ω

- (1) Refer to RETS147X for LF147D and LF147J military specifications.
- (2) Unless otherwise specified the specifications apply over the full temperature range and for V<sub>S</sub>=±20V for the LF147 and for V<sub>S</sub>=±15V for the LF347B/LF347. V<sub>OS</sub>, I<sub>B</sub>, and I<sub>OS</sub> are measured at V<sub>CM</sub>=0.
- (3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T<sub>j</sub>. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P<sub>D</sub>. T<sub>j</sub>=T<sub>A</sub>+θ<sub>JA</sub> P<sub>D</sub> where θ<sub>JA</sub> is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**DC Electrical Characteristics <sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A <sub>VOL</sub>	Large Signal Voltage Gain	V <sub>S</sub> =±15V, T <sub>A</sub> =25°C V <sub>O</sub> =±10V, R <sub>L</sub> =2 kΩ Over Temperature	50	100		50	100		25	100		V/mV
			25			25			15			V/mV
V <sub>O</sub>	Output Voltage Swing	V <sub>S</sub> =±15V, R <sub>L</sub> =10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V <sub>CM</sub>	Input Common-Mode Voltage Range	V <sub>S</sub> =±15V	±11	+15		±11	+15		±11	+15		V
				-12			-12			-12		V
CMRR	Common-Mode Rejection Ratio	R <sub>S</sub> ≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	See <sup>(4)</sup>	80	100		80	100		70	100		dB
I <sub>S</sub>	Supply Current			7.2	11		7.2	11		7.2	11	mA

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V<sub>S</sub> = ± 5V to ±15V for the LF347 and LF347B and from V<sub>S</sub> = ±20V to ±5V for the LF147.

**AC Electrical Characteristics <sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T <sub>A</sub> =25°C, f=1 Hz–20 kHz (Input Referred)		-120			-120			-120		dB
SR	Slew Rate	V <sub>S</sub> =±15V, T <sub>A</sub> =25°C	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	V <sub>S</sub> =±15V, T <sub>A</sub> =25°C	2.2	4		2.2	4		2.2	4		MHz
e <sub>n</sub>	Equivalent Input Noise Voltage	T <sub>A</sub> =25°C, R <sub>S</sub> =100Ω, f=1000 Hz		20			20			20		nV / √Hz
i <sub>n</sub>	Equivalent Input Noise Current	T <sub>J</sub> =25°C, f=1000 Hz		0.01			0.01			0.01		pA / √Hz
THD	Total Harmonic Distortion	A <sub>V</sub> =+10, R <sub>L</sub> =10k, V <sub>O</sub> =20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02			<0.02		%

(1) Unless otherwise specified the specifications apply over the full temperature range and for V<sub>S</sub>=±20V for the LF147 and for V<sub>S</sub>=±15V for the LF347B/LF347. V<sub>OS</sub>, I<sub>B</sub>, and I<sub>OS</sub> are measured at V<sub>CM</sub>=0.

(2) Refer to RETS147X for LF147D and LF147J military specifications.

Typical Performance Characteristics

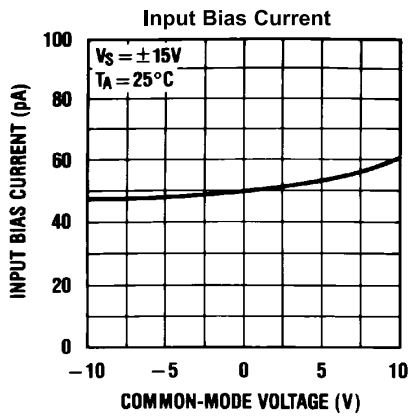


Figure 2.

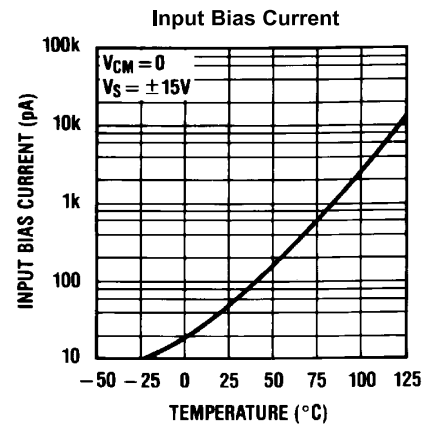


Figure 3.

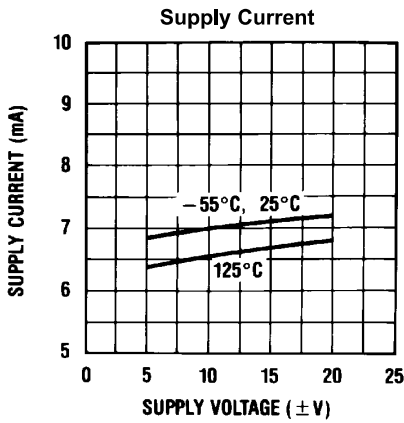


Figure 4.

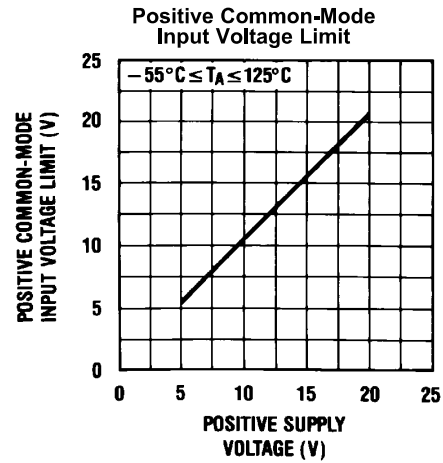


Figure 5.

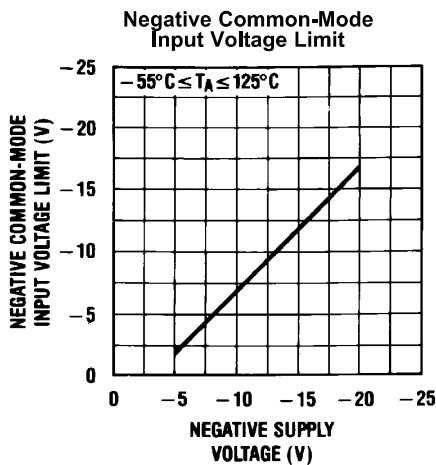


Figure 6.

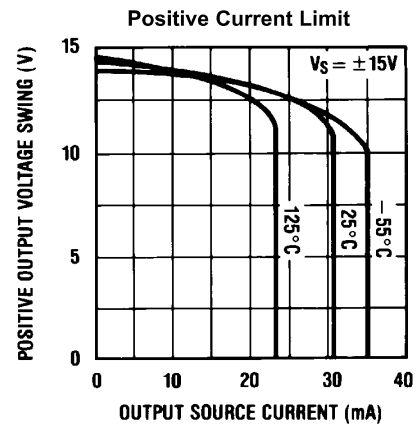


Figure 7.

Typical Performance Characteristics (continued)

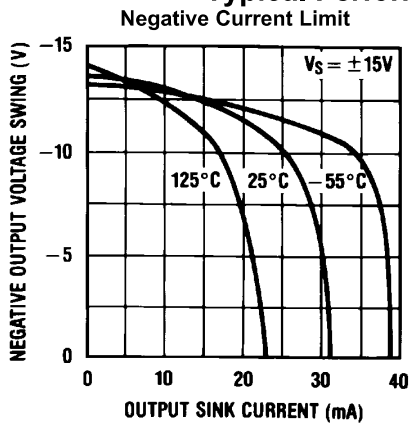


Figure 8.

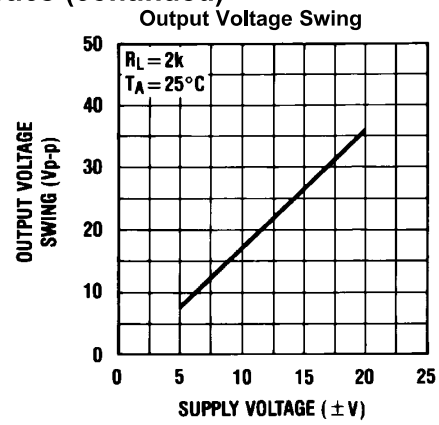


Figure 9.

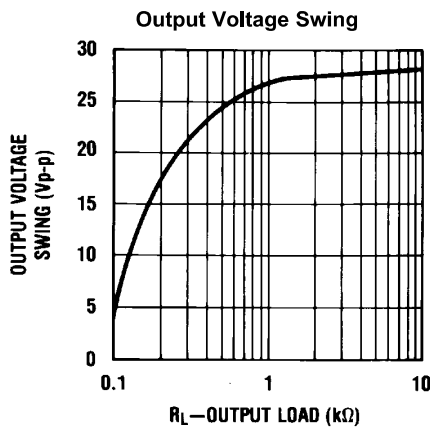


Figure 10.

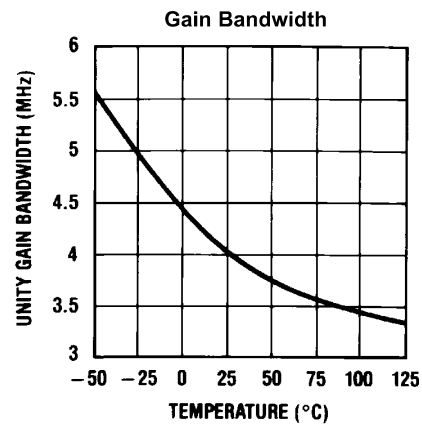


Figure 11.

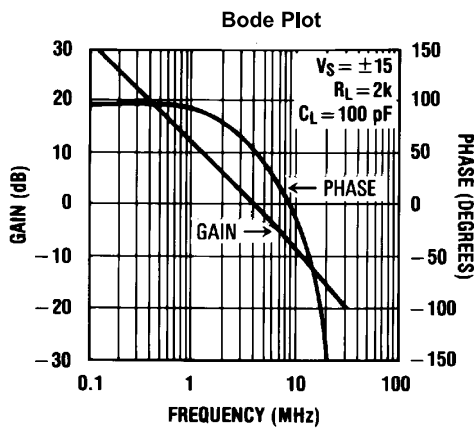


Figure 12.

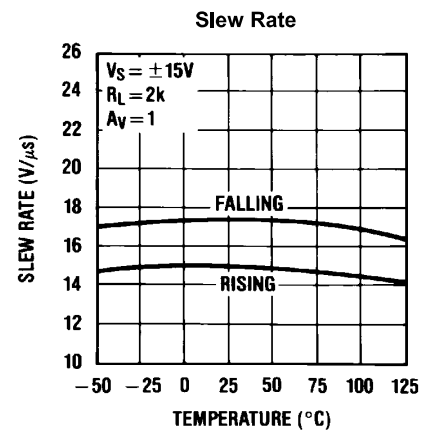
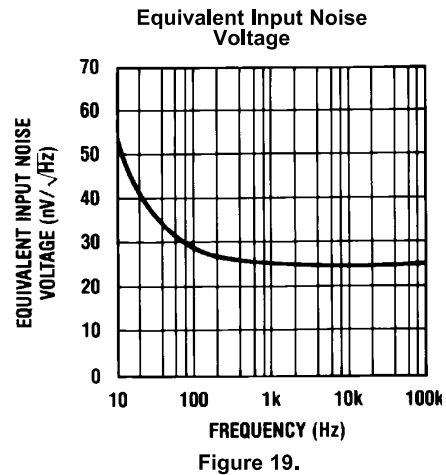
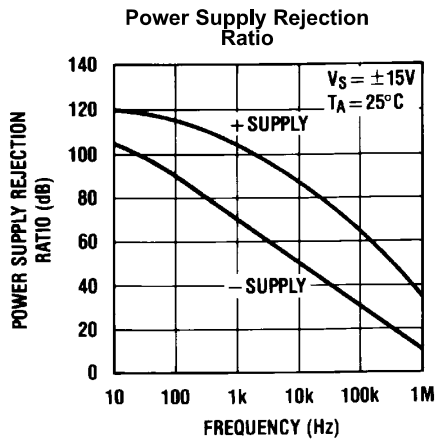
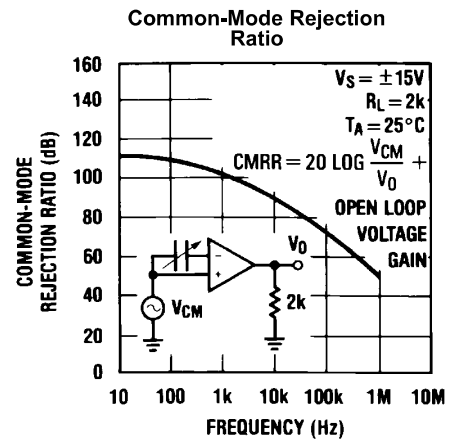
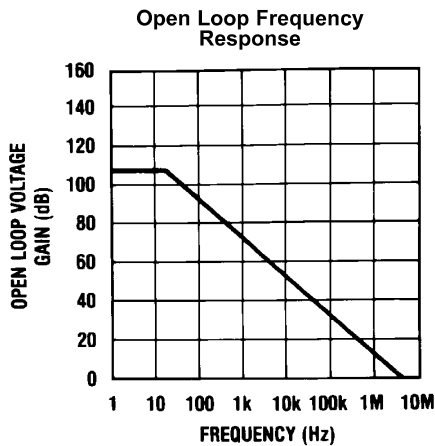
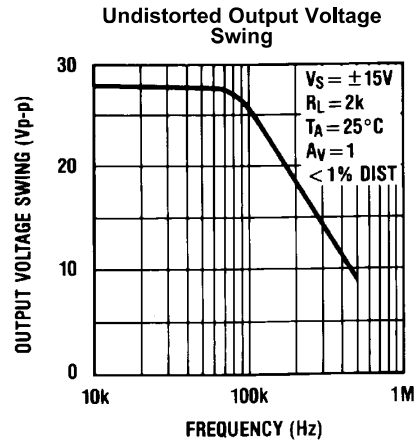
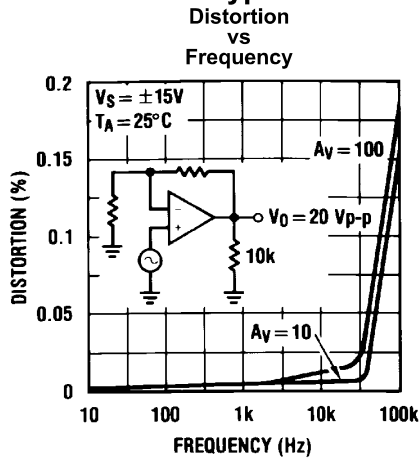
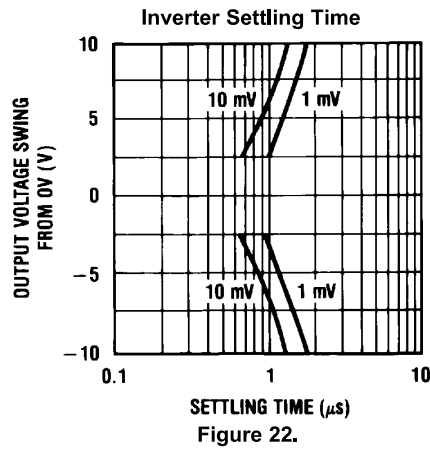
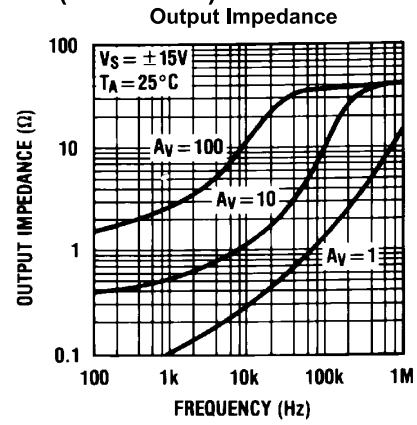
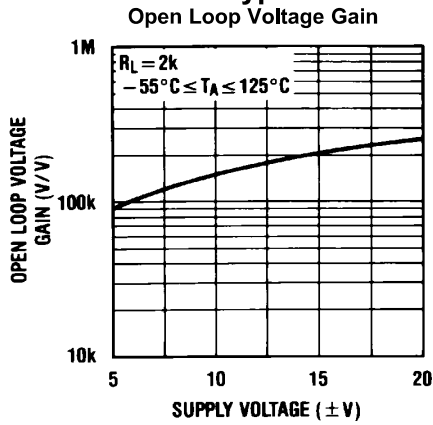


Figure 13.

Typical Performance Characteristics (continued)



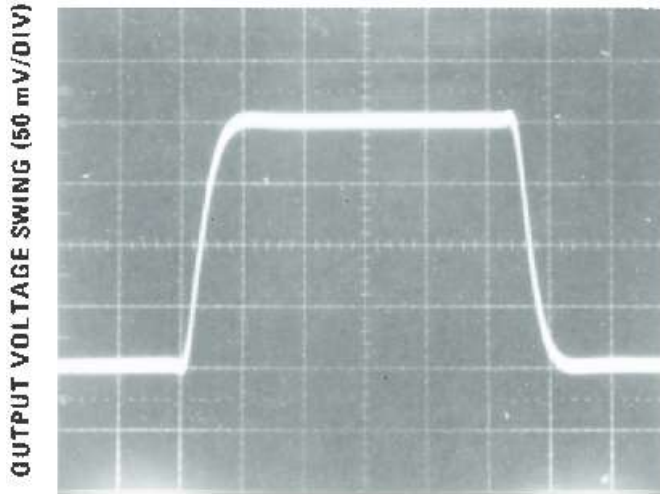
Typical Performance Characteristics (continued)



**Pulse Response**

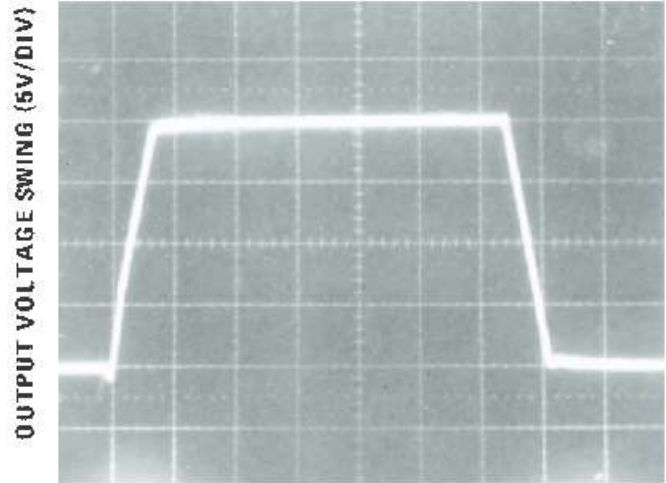
$R_L=2\text{ k}\Omega$ ,  $C_L=10\text{ pF}$

**Small Signal Inverting**



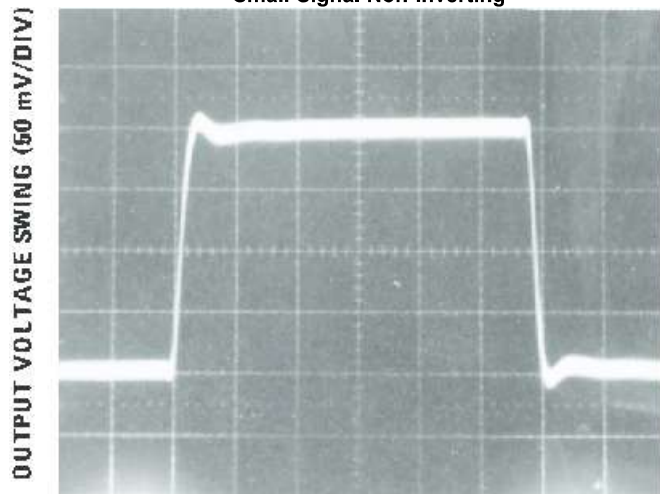
TIME (0.2  $\mu\text{s/DIV}$ )

**Large Signal Inverting**



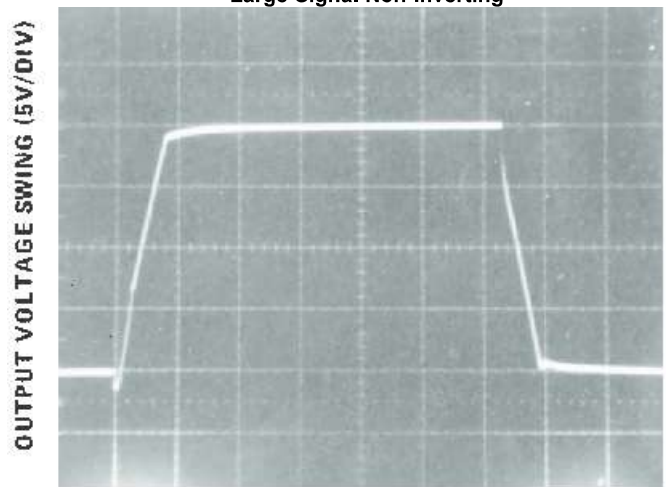
TIME (2  $\mu\text{s/DIV}$ )

**Small Signal Non-Inverting**



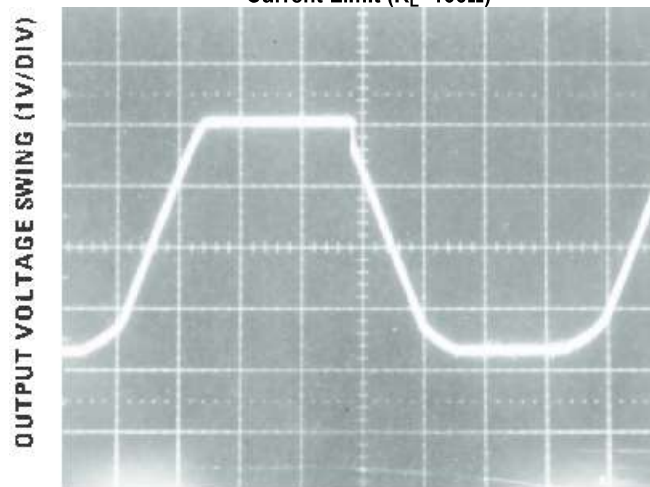
TIME (0.2  $\mu\text{s/DIV}$ )

**Large Signal Non-Inverting**



TIME (2  $\mu\text{s/DIV}$ )

**Current Limit ( $R_L=100\Omega$ )**



TIME (5  $\mu\text{s/DIV}$ )



## APPLICATION HINTS

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on  $\pm 4.5\text{V}$  power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

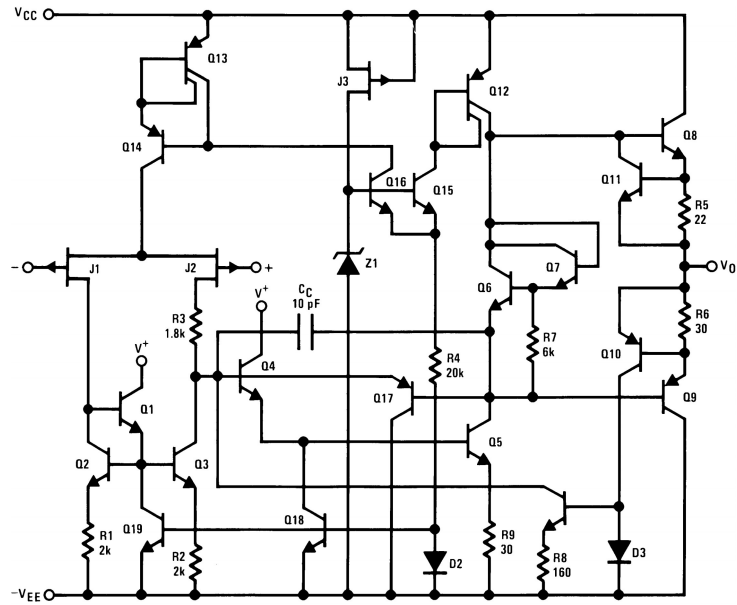
The LF147 will drive a 2 k $\Omega$  load resistance to  $\pm 10\text{V}$  over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

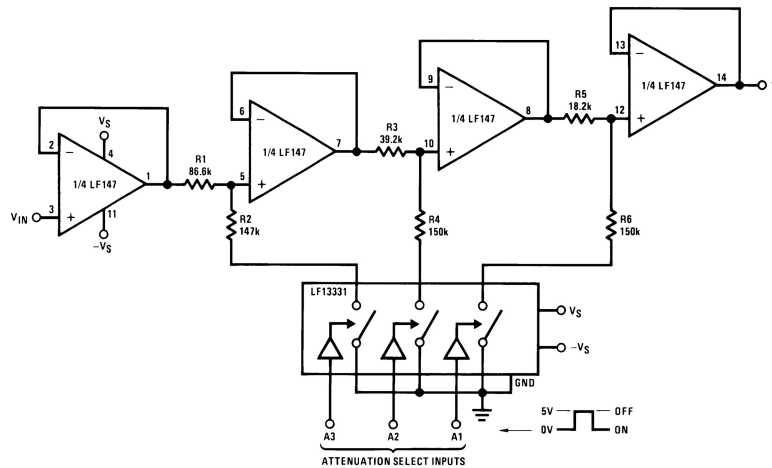
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Figure 23. Digitally Selectable Precision Attenuator

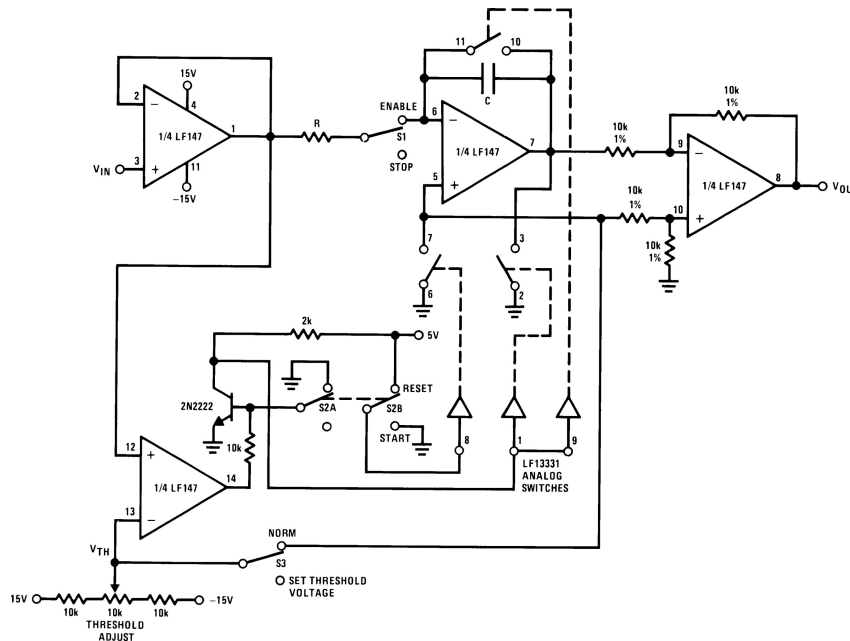


All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors  
No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V <sub>O</sub> Attenuation
0	0	0	0
0	0	1	-1 dB
0	1	0	-2 dB
0	1	1	-3 dB
1	0	0	-4 dB
1	0	1	-5 dB
1	1	0	-6 dB
1	1	1	-7 dB

Figure 24. Long Time Integrator with Reset, Hold and Starting Threshold Adjustment

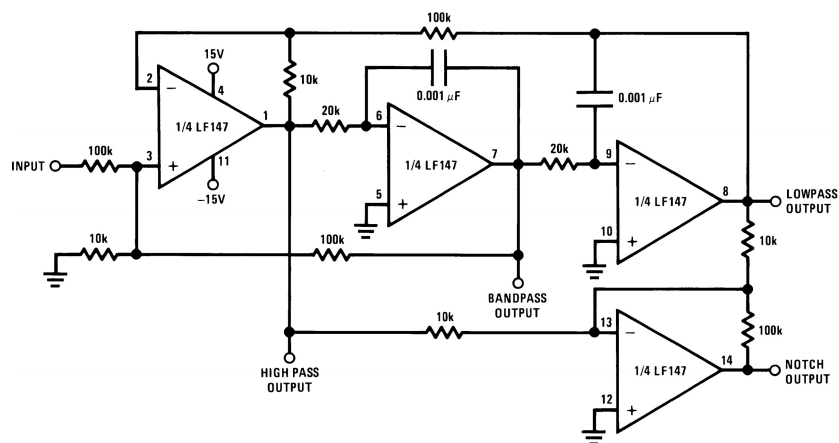


- $V_{OUT}$  starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$

- Output starts when  $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Figure 25. Universal State Variable Filter



For circuit shown:

$f_0 = 3$  kHz,  $f_{NOTCH} = 9.5$  kHz

$Q = 3.4$

Passband gain:

Highpass—0.1

Bandpass—1

Lowpass—1

Notch—10

- $f_0 \times Q \leq 200$  kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

---

**REVISION HISTORY**

<b>Changes from Revision C (March 2013) to Revision D</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">12</a>

---