TEXAS INSTRUMENTS

TL081, TL081A, TL081B, TL082, TL082A
TL082B, TL084, TL084A, TL084B

SLOS081I – FEBRUARY 1977 – REVISED MAY 2015

TL08xx JFET-Input Operational Amplifiers

1 Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs Typical
- Common-Mode Input Voltage Range Includes V_{CC+}

2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

3 Description

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

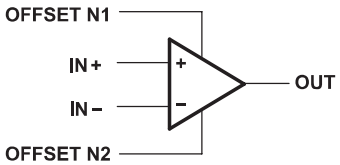
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL084xD	SOIC (14)	8.65 mm × 3.91 mm
TL08xxFK	LCCC (20)	8.89 mm × 8.89 mm
TL084xJ	CDIP (14)	19.56 mm × 6.92 mm
TL084xN	PDIP (14)	19.3 mm × 6.35 mm
TL084xNS	SO (14)	10.3 mm × 5.3 mm
TL084xPW	TSSOP (14)	5.0 mm × 4.4 mm

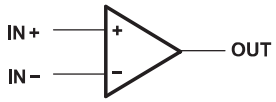
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Symbol

TL081



TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2014) to Revision I — **Page**

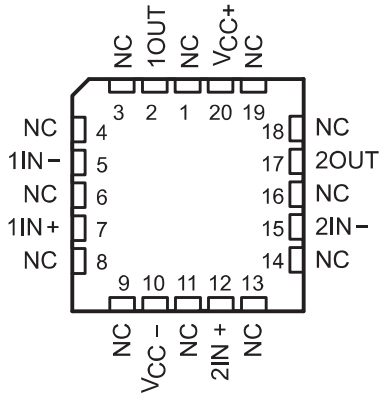
- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Applications* ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 9

Changes from Revision G (September 2004) to Revision H — **Page**

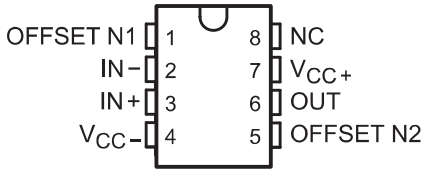
- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

5 Pin Configuration and Functions

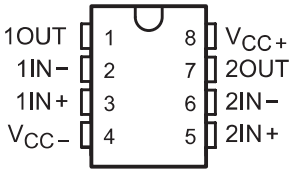
TL082 FK Package
20-Pin LCCC
Top View



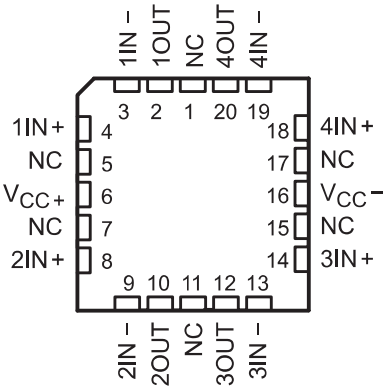
TL081 and TL081x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View



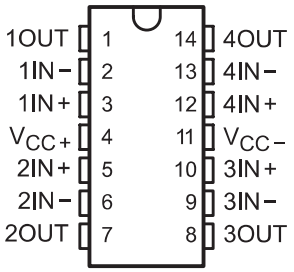
TL082 and TL082x D, JG, P, PS and PW Package
8-Pin SOIC, CDIP, PDIP, SO, and TSSOP
Top View



TL084 FK Package
20-Pin LCCC
Top View



TL084 and TL084x D, J, N, NS and PW Package
14-Pin SOIC, CDIP, PDIP, SO, and TSSOP
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	TL081	TL082		TL084			
	SOIC, PDIP, SO	SOIC, CDIP, PDIP, SO, TSSOP	LCCC	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
1IN–	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN–	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN–	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN–	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output

Pin Functions (continued)

PIN						I/O	DESCRIPTION
NAME	TL081	TL082		TL084			
	SOIC, PDIP, SO	SOIC, CDIP, PDIP, SO, TSSOP	LCCC	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
IN–	2	—	—	—	—	I	Negative input
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3				
			4		5		
			6				
			8		7		
			9				
			11		11		
			13				
			14		15		
			16				
			18		17		
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
V_{CC-}	4	4	10	11	16	—	Power supply
V_{CC+}	7	8	20	4	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)				18	V
V_{CC-}					–18	
V_{ID}	Differential input voltage(3)				±30	V
V_I	Input voltage(2)(4)				±15	V
	Duration of output short circuit(5)			Unlimited		
	Continuous total power dissipation			See *Dissipation Rating Table*		
T_A	Operating free-air temperature		TL08_C TL08_AC TL08_BC	0	70	°C
			TL08_I	–40	85	
			TL084Q	–40	125	
			TL08_M	–55	125	
	Operating virtual junction temperature				150	°C
T_C	Case temperature for 60 seconds	FK package	TL08_M		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package	TL08_M		300	°C
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Ambient temperature	TL08xM	–55	125	°C
		TL08xQ	–40	125	
		TL08xI	–40	85	
		TL08xC	0	70	

6.4 Thermal Information

THERMAL METRIC[1]		TL08xx								UNIT
		D (SOIC)		N (PDIP)	NS (SO)	P (PDIP)	PS (SO)	PW (TSSOP)		
		8 PINS	14 PINS	14 PINS	14 PINS	{PIN COUNT} PINS	{PIN COUNT} PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2][3]	97	86	76	80	85	95	149	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC±}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[1]	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current[2]	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current[2]	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

Electrical Characteristics for TL08xC, TL08xxC, and TL08xI (continued)

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

6.6 Electrical Characteristics for TL08xM and TL084x

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current (2)	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current (2)	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
			Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

6.7 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19	8 (1)	13		V/µs
		V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, T_A = – 55°C to 125°C, See Figure 19	5 (1)			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Operating Characteristics (continued)

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise-time	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19			0.05		µs
	overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ, f = 1 kHz,			0.003%		

6.8 Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in *Parameter Measurement Information*.

Table 1. Table of Graphs

			Figure
V_{OM}	Maximum peak output voltage	versus Frequency versus Free-air temperature versus Load resistance versus Supply voltage	Figure 1, Figure 2, Figure 3 Figure 4 Figure 5 Figure 6
A_{VD}	Large-signal differential voltage amplification	versus Free-air temperature versus Load resistance	Figure 7 Figure 8
	Differential voltage amplification	versus Frequency with feed-forward compensation	Figure 9
P_D	Total power dissipation	versus Free-air temperature	Figure 10
I_{CC}	Supply current	versus Free-air temperature versus Supply voltage	Figure 11 Figure 12
I_{IB}	Input bias current	versus Free-air temperature	Figure 13
	Large-signal pulse response	versus Time	Figure 14
V_O	Output voltage	versus Elapsed time	Figure 15
CMRR	Common-mode rejection ratio	versus Free-air temperature	Figure 16
V_n	Equivalent input noise voltage	versus Frequency	Figure 17
THD	Total harmonic distortion	versus Frequency	Figure 18

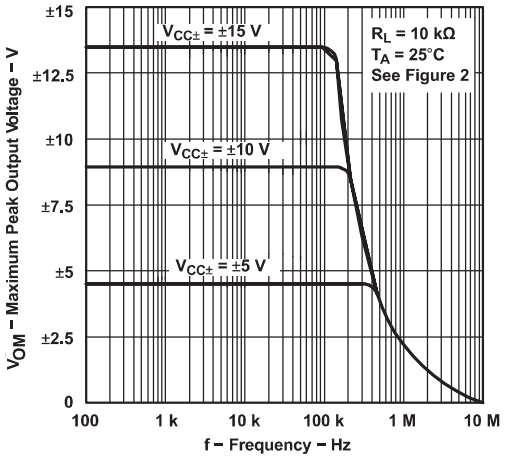


Figure 1. Maximum Peak Output Voltage vs Frequency

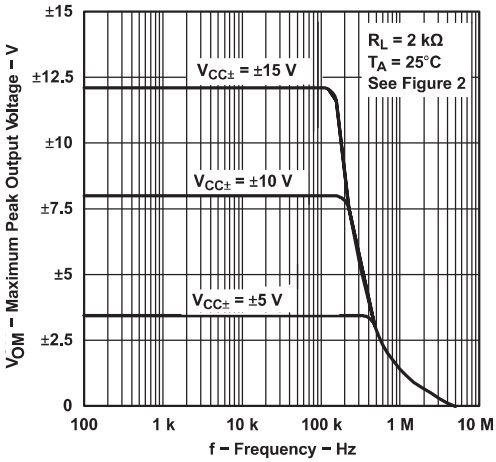


Figure 2. Maximum Peak Output Voltage vs Frequency

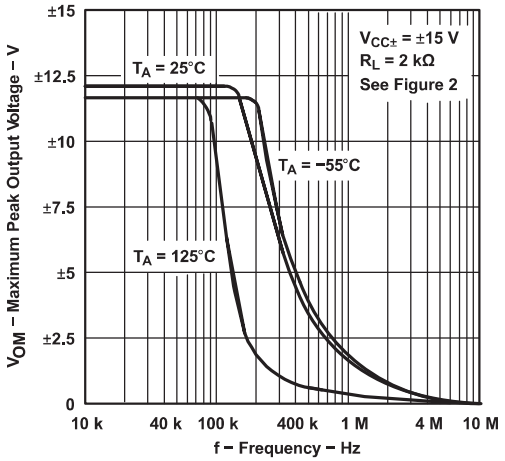


Figure 3. Maximum Peak Output Voltage vs Frequency

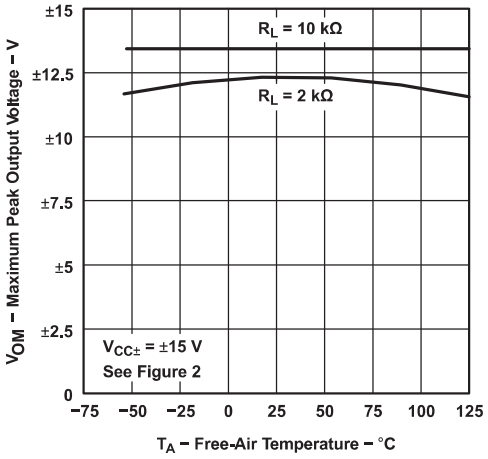


Figure 4. Maximum Peak Output Voltage vs Free-Air Temperature

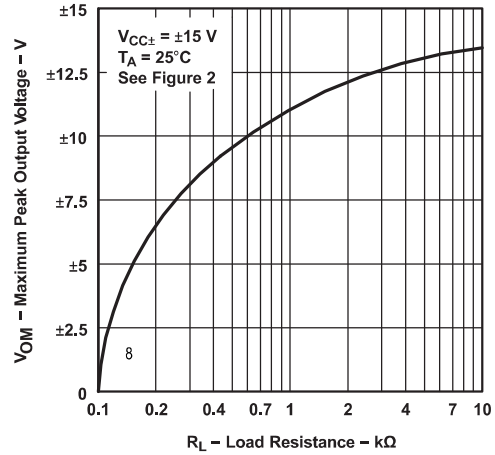


Figure 5. Maximum Peak Output Voltage vs Load Resistance

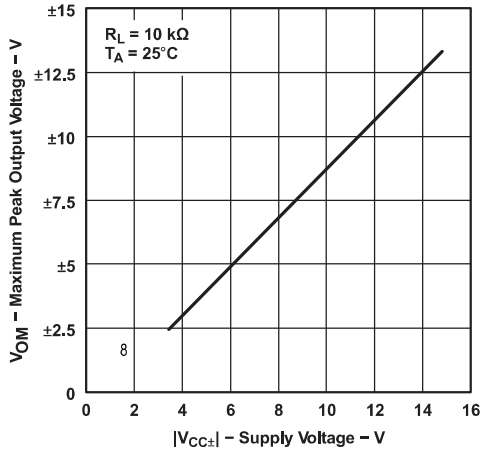


Figure 6. Maximum Peak Output Voltage vs Supply Voltage

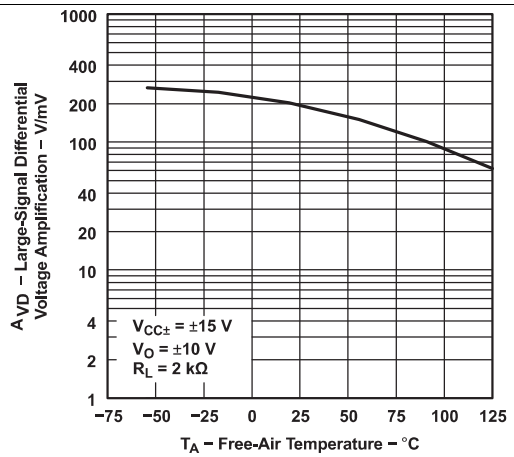


Figure 7. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

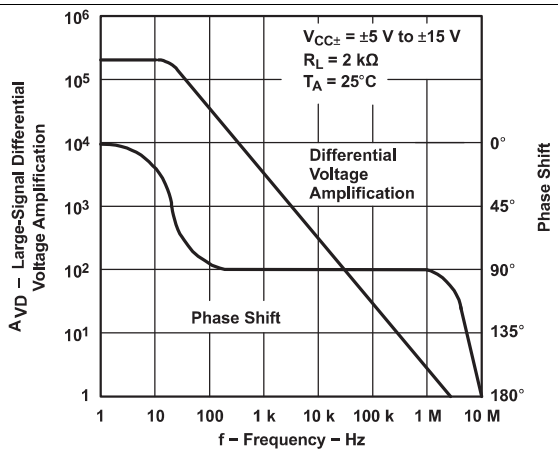


Figure 8. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

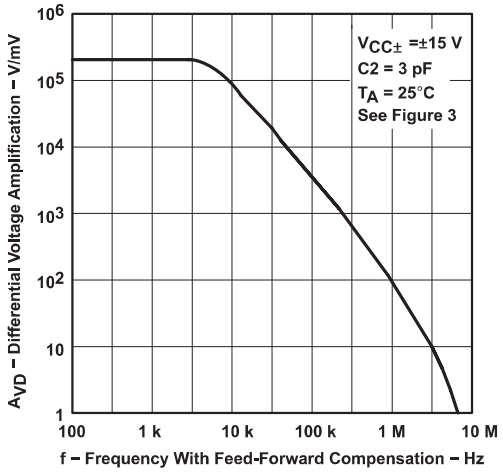


Figure 9. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation

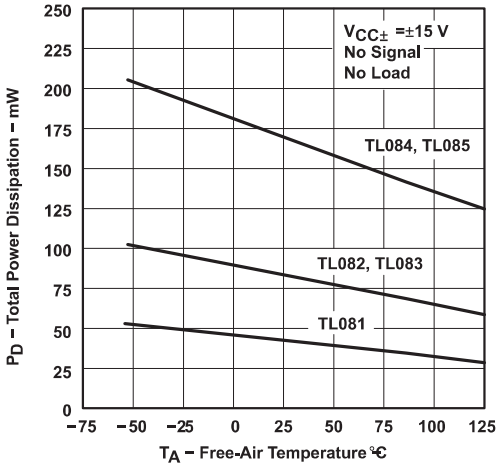


Figure 10. Total Power Dissipation vs Free-Air Temperature

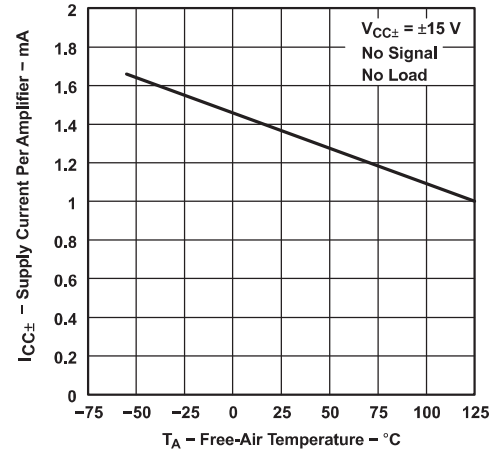


Figure 11. Supply Current per Amplifier vs Free-Air Temperature

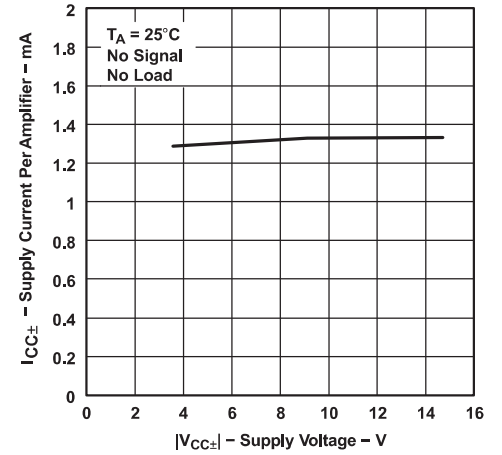


Figure 12. Supply Current per Amplifier vs Supply Voltage

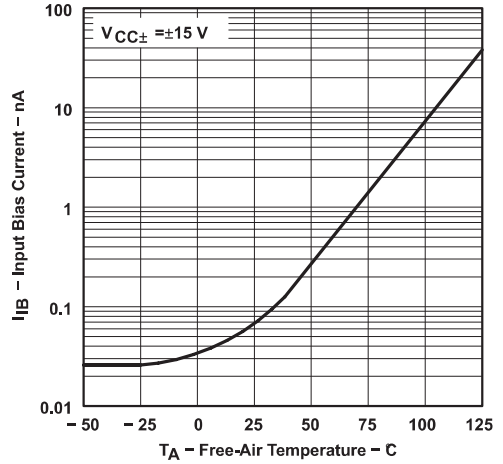


Figure 13. Input Bias Current vs Free-Air Temperature

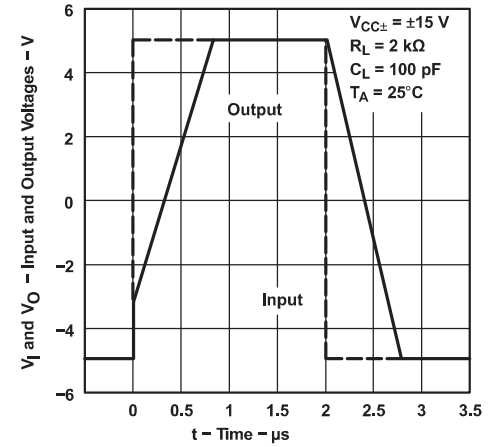


Figure 14. Voltage-Follower Large-Signal Pulse Response

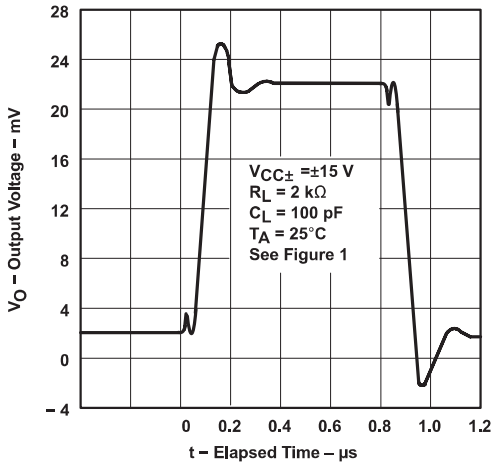


Figure 15. Output Voltage vs Elapsed Time

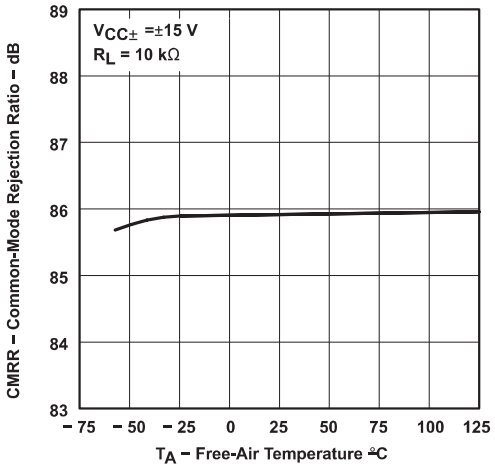


Figure 16. Common-Mode Rejection Ratio vs Free-Air Temperature

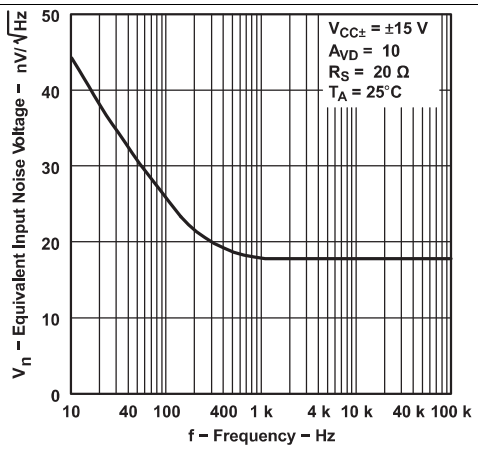


Figure 17. Equivalent Input Noise Voltage vs Frequency

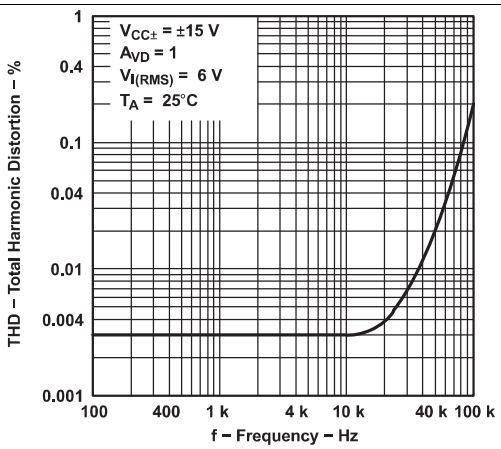


Figure 18. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

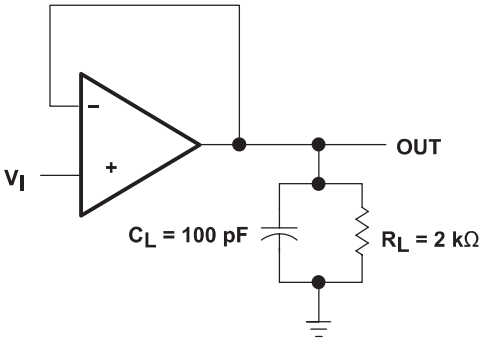


Figure 19. Test Figure 1

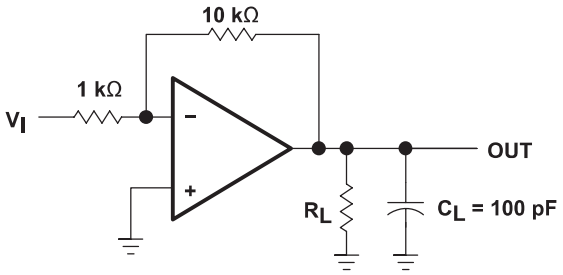


Figure 20. Test Figure 2

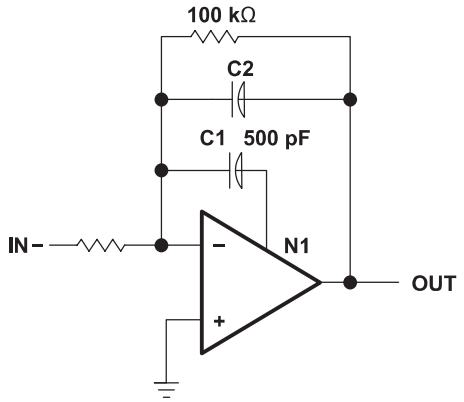


Figure 21. Test Figure 3

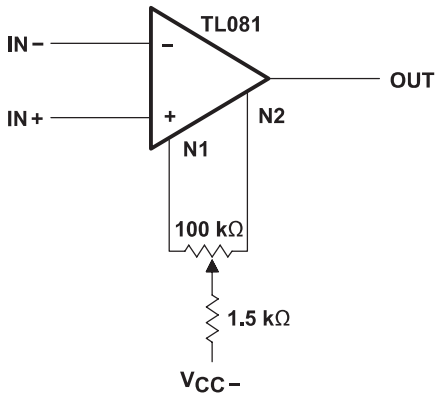


Figure 22. Test Figure 4

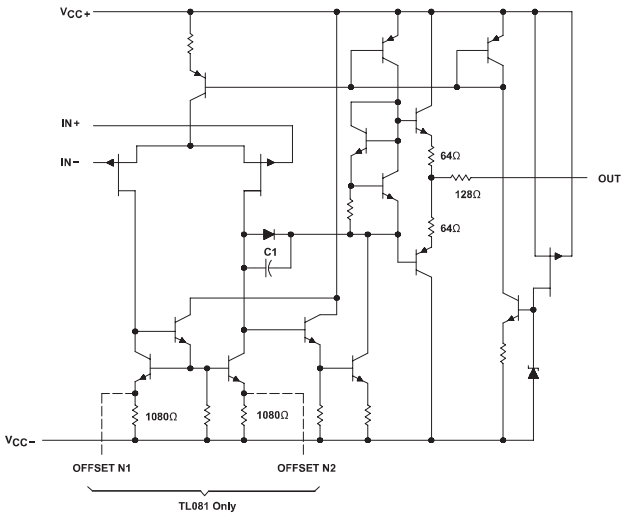
8 Detailed Description

8.1 Overview

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08xx family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to +125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

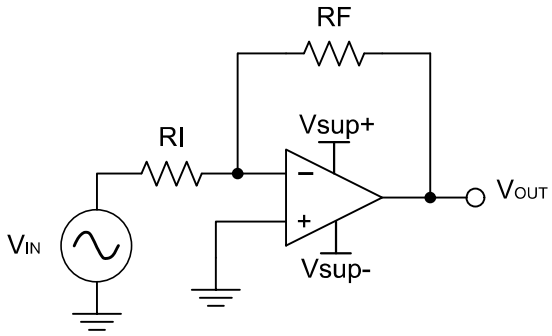


Figure 23. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

Typical Applications (continued)

9.2.1.3 Application Curve

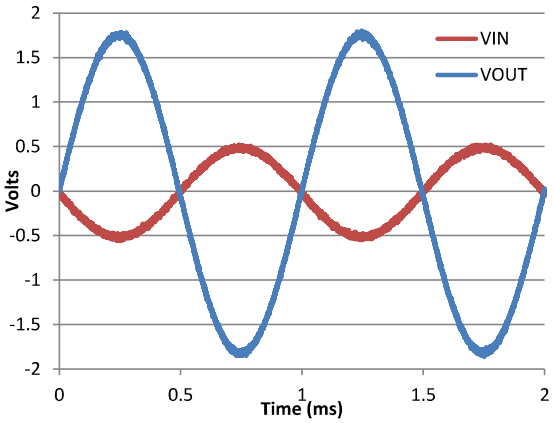


Figure 24. Input and output voltages of the inverting amplifier

9.3 System Examples

9.3.1 General Applications

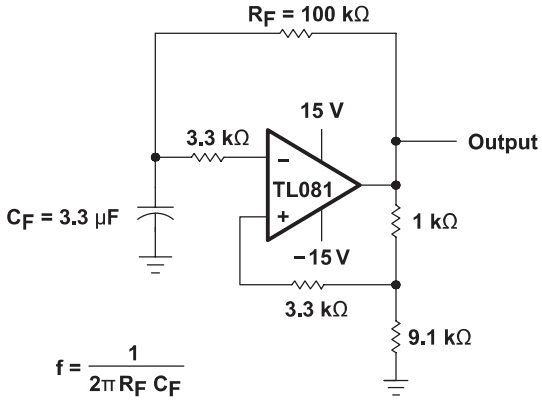


Figure 25. 0.5-Hz Square-Wave Oscillator

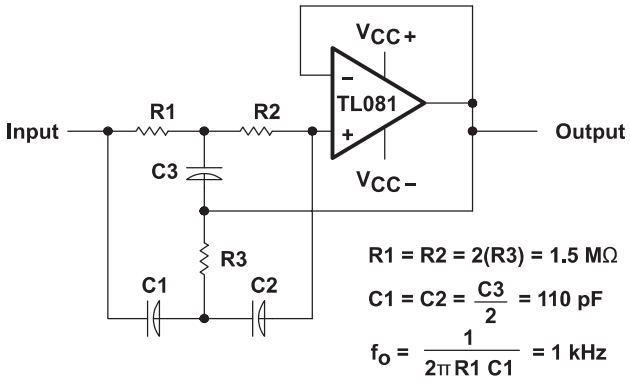


Figure 26. High-Q Notch Filter

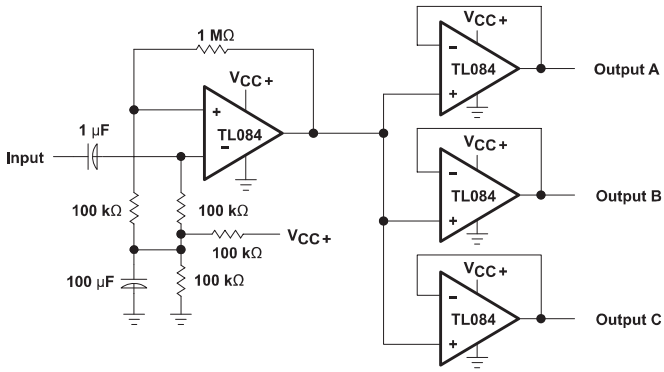
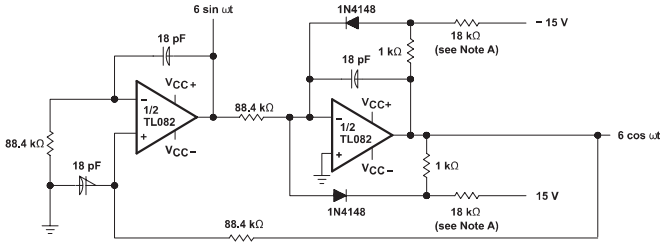


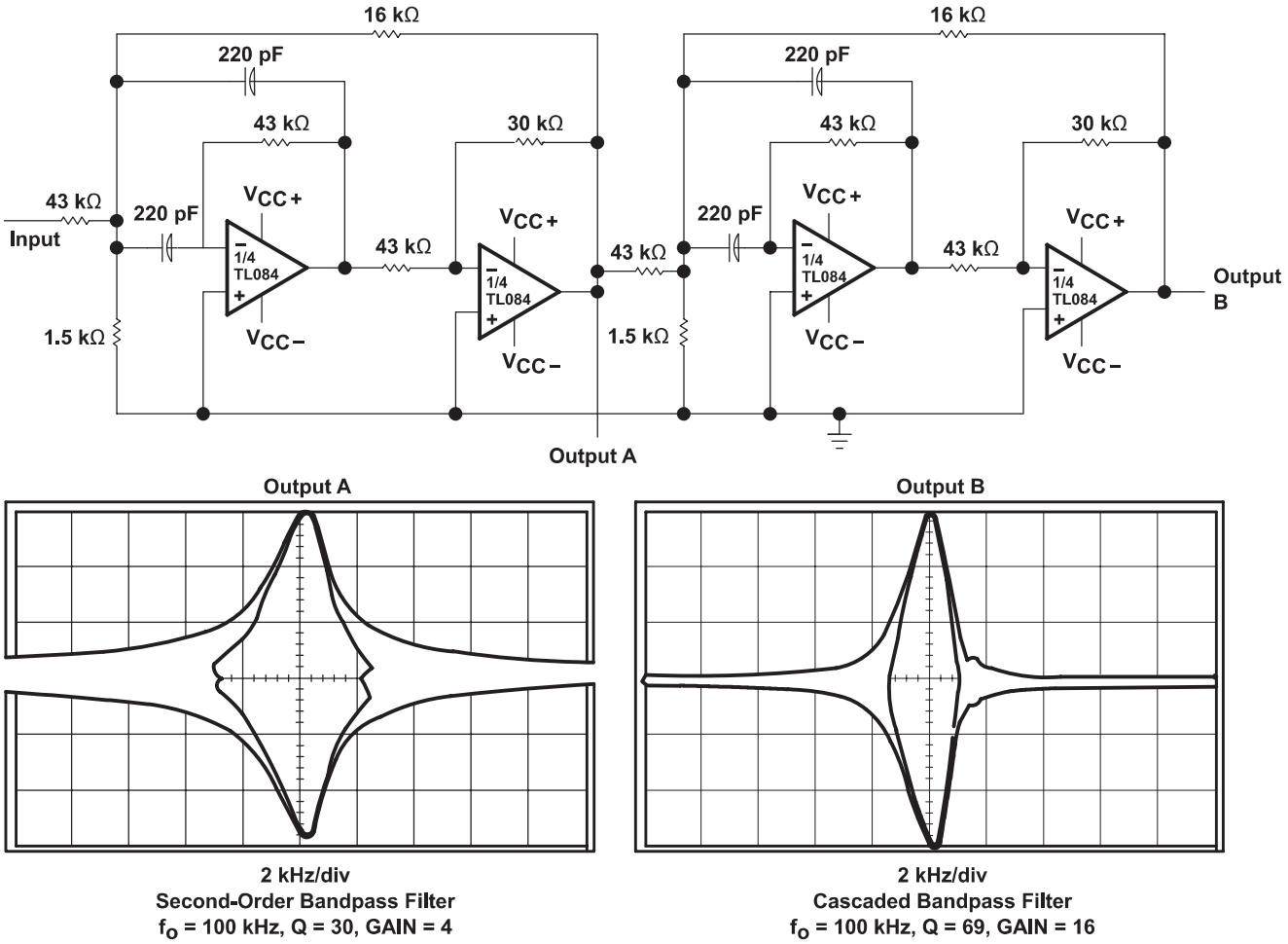
Figure 27. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 28. 100-kHz Quadrature Oscillator

System Examples (continued)



2 kHz/div
Second-Order Bandpass Filter
f_O = 100 kHz, Q = 30, GAIN = 4

2 kHz/div
Cascaded Bandpass Filter
f_O = 100 kHz, Q = 69, GAIN = 16

Figure 29. Positive-Feedback Bandpass Filter

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

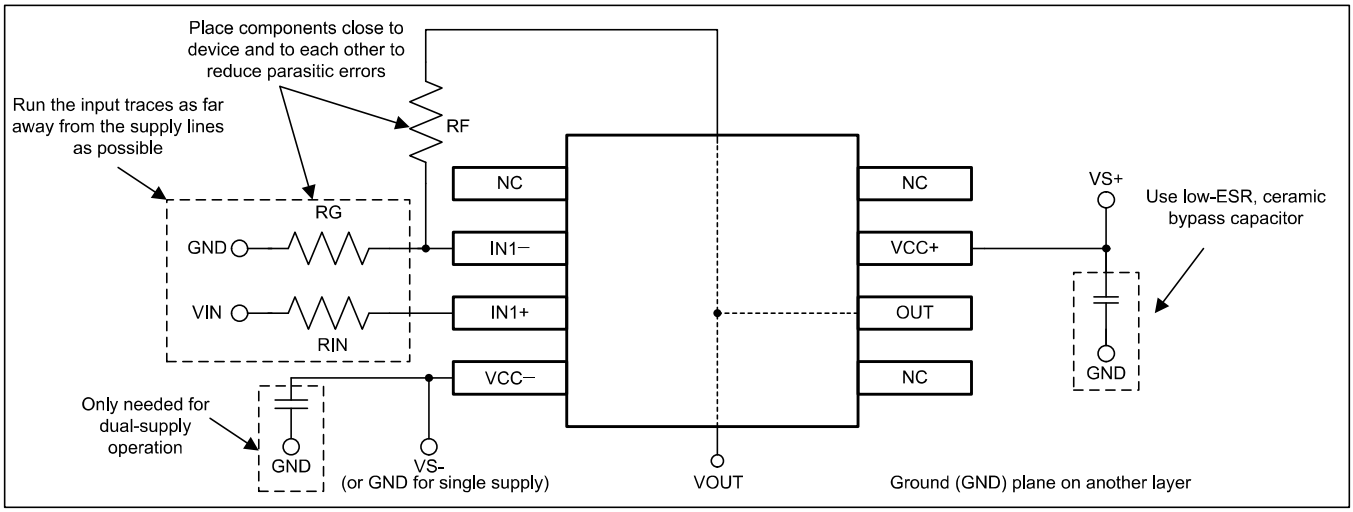


Figure 30. Operational Amplifier Board Layout for Noninverting Configuration

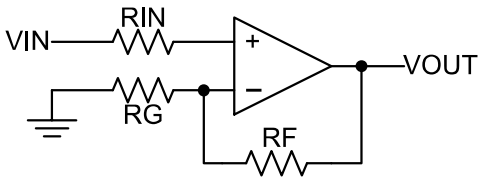


Figure 31. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For more information, see the following:

- *Circuit Board Layout Techniques*, SLOA089.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL081	Click here	Click here	Click here	Click here	Click here
TL081A	Click here	Click here	Click here	Click here	Click here
TL081B	Click here	Click here	Click here	Click here	Click here
TL082	Click here	Click here	Click here	Click here	Click here
TL082A	Click here	Click here	Click here	Click here	Click here
TL082B	Click here	Click here	Click here	Click here	Click here
TL084	Click here	Click here	Click here	Click here	Click here
TL084A	Click here	Click here	Click here	Click here	Click here
TL084B	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.