Am2506

Four-Bit Arithmetic Logic Unit/Function Generator with Output Latch

Distinctive Characteristics:

- Provides 16 arithmetic operations including add, subtract, double and compare.
- Provides ALL 16 possible logic operations of two variables in typically 22 ns.
- Output latch provided to hold contents of operation.
- Typical add time for 4 bits of only 22 ns, and typical carry time of 12 ns.
- Full Look-ahead for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am2506 is a 4-bit high-speed parallel Arithmeic Logic Unit (ALU)/ Digital Function Generator with Output Latch. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

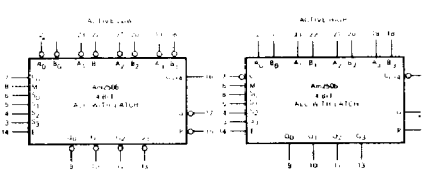
If the latch enable E is held HIGH the result of an operation appears at the outputs Q_0 to Q_3 and is stored in the latch when E goes LOW.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate (P) and carry generate (G) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am2506 ALU's and one Am54/74182 look-ahead generator is only 34 ns.

For systems where ultra high-speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple-block arithmetic operations.

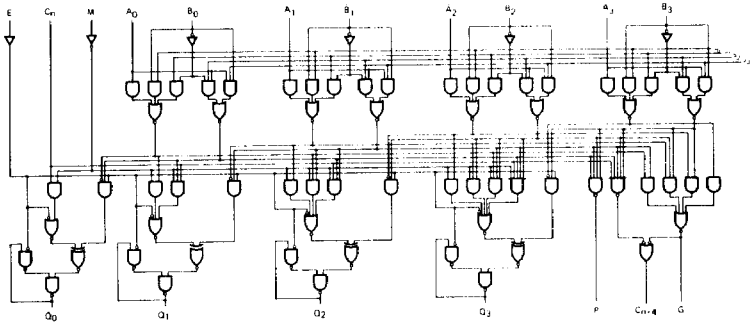
The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode by reinterpreting the carry signals.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

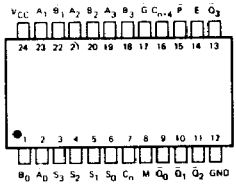


Am2506 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM250659C
Hermetic DIP	0°C to +75°C	AM250659G
Hermetic DIP	−55°C to +125°C	AM250651G
Hermetic Flat Pak	−55°C to +125°C	AM250651P
Dice	Note	AM2506XXD

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATI (Above which the useful life may be impaired)

Storage Temperature	−65°C to +15
Temperature (Ambient) Under Bias	−55°C to +12
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} I
DC Input Voltage	−0.5 V to +5
Output Current, Into Outputs	30
DC Input Current	−30 mA to +5

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am250659X — T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am250651X — T_A = −55°C to +125°C V_{CC} = 4.5 V to 5.50 V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current Am250659X	V_{CC} = MAX., V_{OUT} = 0.0 V		−18		−57	mA
I_{SC}	Output Short Circuit Current Am250651X	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−55	mA
I_{CC}	Power Supply Current Am250651X	V_{CC} = MAX.	A_{0-3} = 4.5 V B_{0-3}, C_n = 0 V		88	127	mA
			A_{0-3}, B_{0-3}, C_n = 0 V		94	135	
I_{CC}	Power Supply Current Am250659X	V_{CC} = MAX.	A_{0-3} = 4.5 V B_{0-3}, C_n = 0 V		88	140	mA
			A_{0-3}, B_{0-3}, C_n = 0 V		94	150	

Note 1. Typical limits are at Vcc = 5.0 V, 25°C ambient and maximum loading.
Note 2. For other input currents use Am2506 loading rules.

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

Parameter	From	To	Test Conditions See also Tables 1, 2, 3	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		8	12	18	ns
t_{pd-}				8	13	19	
t_{pd+}	C_n	$\overline{Q}_i$	M = 0 V, E = 4.5 V (SUM or DIFF mode)	8	15	19	ns
t_{pd-}				8	13	18	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_1 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	8	13	19	ns
t_{pd-}				8	13	19	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_1 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	11	17	25	ns
t_{pd-}				11	17	25	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_1 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	8	15	19	ns
t_{pd-}				8	15	22	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_1 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	11	17	25	ns
t_{pd-}				11	17	25	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_1 = 4.5 V, E = 4.5 V S_1 = S_2 = 0 V (SUM mode)	14	22	29	ns
t_{pd-}				14	21	30	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_1 = 0 V, E = 4.5 V S_1 = S_2 = 4.5 V (DIFF mode)	17	27	36	ns
t_{pd-}				15	23	32	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_i$	M = 4.5 V (LOGIC mode), E = 4.5 V	14	22	29	ns
t_{pd-}				14	22	29	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_1 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	11	17	25	ns
t_{pd-}				14	20	30	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_1 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	14	21	32	ns
t_{pd-}				14	20	30	
t_{pd+}	Enable LOW to HIGH	$\overline{Q}_i$	M = 0 V, S_0 = S_1 = 4.5 V S_1 = S_2 = 0 V (SUM mode)	8	15	23	ns
t_{pd-}				7	14	21	
t_w(E)	Minimum Enable HIGH Time		M = 0 V, S_0 = S_1 = 4.5 V S_1 = S_2 = 0 V (SUM mode)		5	10	ns
t_s(E)	Set Up Time, Q Outputs to enable HIGH to LOW			−18		− 8	ns

TEST TABLES

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = E = 4.5\ V$, $S_0 = S_3 = M = 0\ V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{Q}_{i+1}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}	1

Table 1

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = E = 4.5\ V$, $S_1 = S_2 = M = 0\ V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{Q}$ or C_{n+4}	1

Table 2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5\ V$, $S_0 = S_3 = 0\ V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{Q}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{Q}$	1

Table 3

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{A}_i$ Active LOW Data A inputs $i = 0, 1, 2, 3$.

$\overline{B}_i$ Active LOW Data B inputs $i = 0, 1, 2, 3$.

C_n Active HIGH Carry in to nth ALU bit.

C_{n+4} Active HIGH Carry Out of n+4th ALU bit.

E Active HIGH output latch enable. The result of an operation is stored when the Enable goes from a HIGH Logic level to a LOW Logic level.

$\overline{Q}_i$ Active LOW Data Outputs of ALU latch $i = 0, 1, 2, 3$.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{G}$ Active LOW carry generate output for use in multi-level look-ahead schemes.

M Mode input controls whether arithmetic or logic operation.

$\overline{P}$ Active LOW carry propagate output for use in multi-level look-ahead schemes.

S_i Control inputs determine the arithmetic or logic function obeyed $i = 0, 1, 2, 3$.

Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table 4

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement requires an end around carry.
4. Subtraction in 2's complement arithmetic requires a carry in (C_n = HIGH) active LOW case, ($\overline{C}_n$ = LOW) active HIGH case.
5. In the active HIGH case the B field can be complemented, and in the active LOW case the A field can be complemented. The operation table is changed by complementing the appropriate variable for each operation.

Am2506 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{B}_0$	1	3	—	—
$\overline{A}_0$	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
$\overline{O}_0$	9	—	20	10
$\overline{O}_1$	10	—	20	10
$\overline{O}_2$	11	—	20	10
GND	12	—	—	—
$\overline{O}_3$	13	—	20	10
E	14	1	—	—
$\overline{P}$	15	—	20	10
C_{n+4}	16	—	20	10
$\overline{G}$	17	—	20	10
$\overline{B}_3$	18	3	—	—
$\overline{A}_3$	19	3	—	—
$\overline{B}_2$	20	3	—	—
$\overline{A}_2$	21	3	—	—
$\overline{B}_1$	22	3	—	—
$\overline{A}_1$	23	3	—	—
V_{CC}	24	—	—	—

Table 5

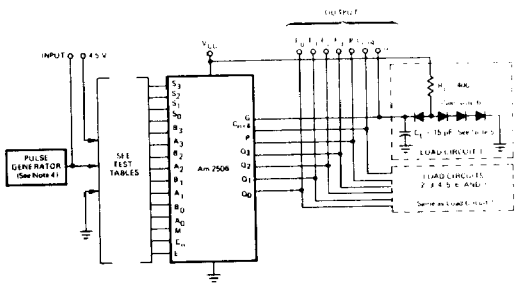
OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0 S_1 S_2 S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L L L L	A minus 1	$\overline{A}$	A	$\overline{A}$
H L L L	AB minus 1	$\overline{AB}$	$A + \overline{B}$	$\overline{A + B}$
L H L L	$A\overline{B}$ minus 1	$\overline{A} + B$	$A + \overline{B}$	$\overline{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus $[A + \overline{B}]$	$\overline{A + B}$	A plus $A\overline{B}$	$\overline{AB}$
H L H L	AB plus $[A + \overline{B}]$	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L H H L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$
H H H L	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L L L H	A plus [A + B]	$\overline{AB}$	A plus AB	$\overline{A} + B$
H L L H	A plus B	$A \oplus B$	A plus B	$\overline{A \oplus B}$
L H L H	$A\overline{B}$ plus $[A + \overline{B}]$	B	AB plus $[A + \overline{B}]$	B
H H L H	A + B	A + B	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus AB	$A\overline{B}$	A plus [A + B]	$A + \overline{B}$
L H H H	A plus $A\overline{B}$	AB	A plus $[A + \overline{B}]$	A + B
H H H H	A	A	A minus 1	A

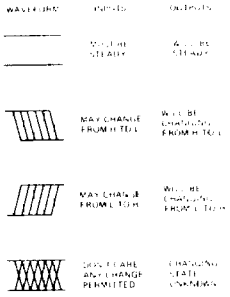
L = LOW Voltage Level
H = HIGH Voltage Level

Table 6

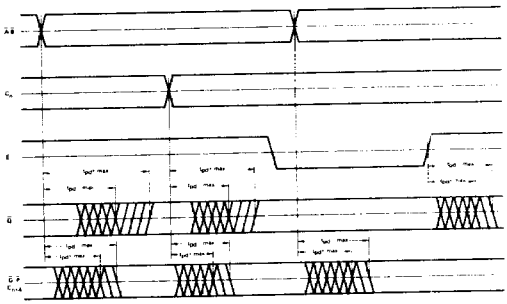
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

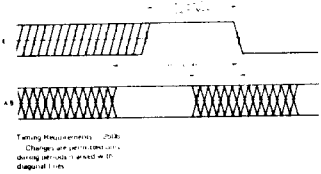


KEY TO TIMING DIAGRAM



Note 4. The pulse generator has the following characteristics: frequency = 1 MHz, $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

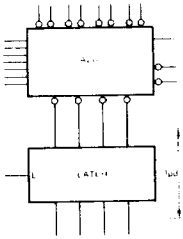




Am2506 SET-UP and RELEASE TIMES

To determine the timing requirements for the enable input of the Am2506, it is helpful to consider the device as consisting of two parts, an ALU followed by a latch on the outputs. See the Figure. (In fact, the latch is an integral part of the ALU and does not contribute delay between the Am2506 inputs and outputs. The latch in the model therefore has a propagation delay of zero.) The delay between input changes on the ALU and steady data on the inputs of the latch is defined by the tpd's of the Am2506. In the model, a signal change on an ALU input will cause the data at the latch input to change sometime between t_{pd} min and t_{pd} max for that path in the Am2506 switching specification. The set-up and release times for the enable input may be defined in the ordinary manner; they are the maximum and minimum set-up times for the data inputs relative to the end of the enable pulse. To guarantee storing data, the data must be present at the latch input for at least t_s max before the end of the enable. To guarantee not storing data, the latch inputs must not change until after t_r min before the end of the enable. The maximum and minimum set-up times for the Am2506 are defined in this fashion for the latch in the model shown.

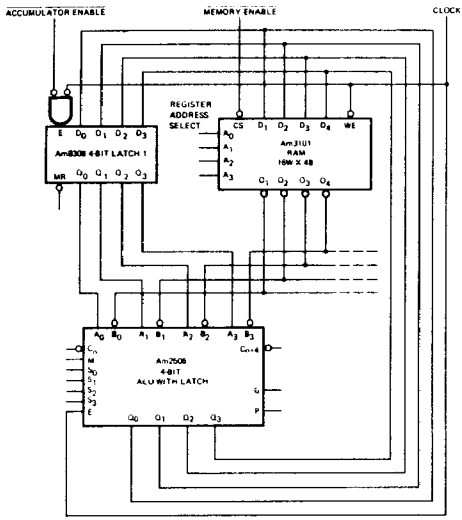
The timing requirements for the Am2506 can then be stated as follows: To guarantee storing data, the time between the application of steady data to the Am2506 inputs and the end of the latch enable must be at least t_{pd} max plus t_s max. To guarantee not storing data, the delay between a change on the Am2506 inputs and the end of the latch enable must be less than t_{pd} min plus t_r min. Since the set-up times are negative, the algebraic addition allows the latch enable to end before the data actually appears at the Am2506 output.



Model of Am2506 With Separate Latch On ALU Outputs

Am2506 APPLICATION

16-WORD 4-BIT ARITHMETIC REGISTER SLICE



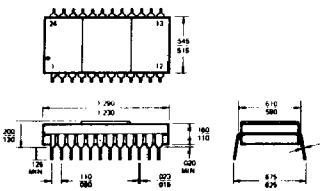
FUNCTION TABLE

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	A + B	$\overline{AB}$
L	H	L	L	A + B	$\overline{A\overline{B}}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus [A + B]	B
L	H	H	L	A plus B	$A \oplus \overline{B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $A\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus [A + B]	$\overline{B}$
H	H	L	H	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus [A + $\overline{B}$]	A + B
L	H	H	H	A plus [A + B]	A + $\overline{B}$
H	H	H	H	A minus 1	A

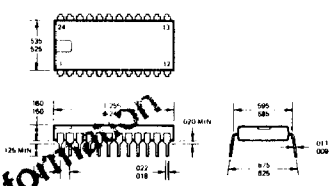
L = Low Voltage Level
H = High Voltage Level

PHYSICAL DIMENSIONS
Dual-In-Line

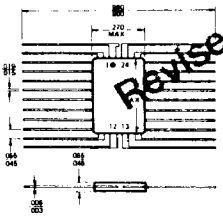
Hermetic



Molded

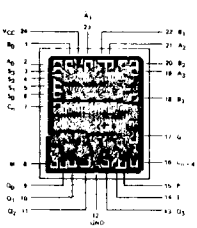


Flat Package



Metallization and Pad Layout

90 x 108 Mils



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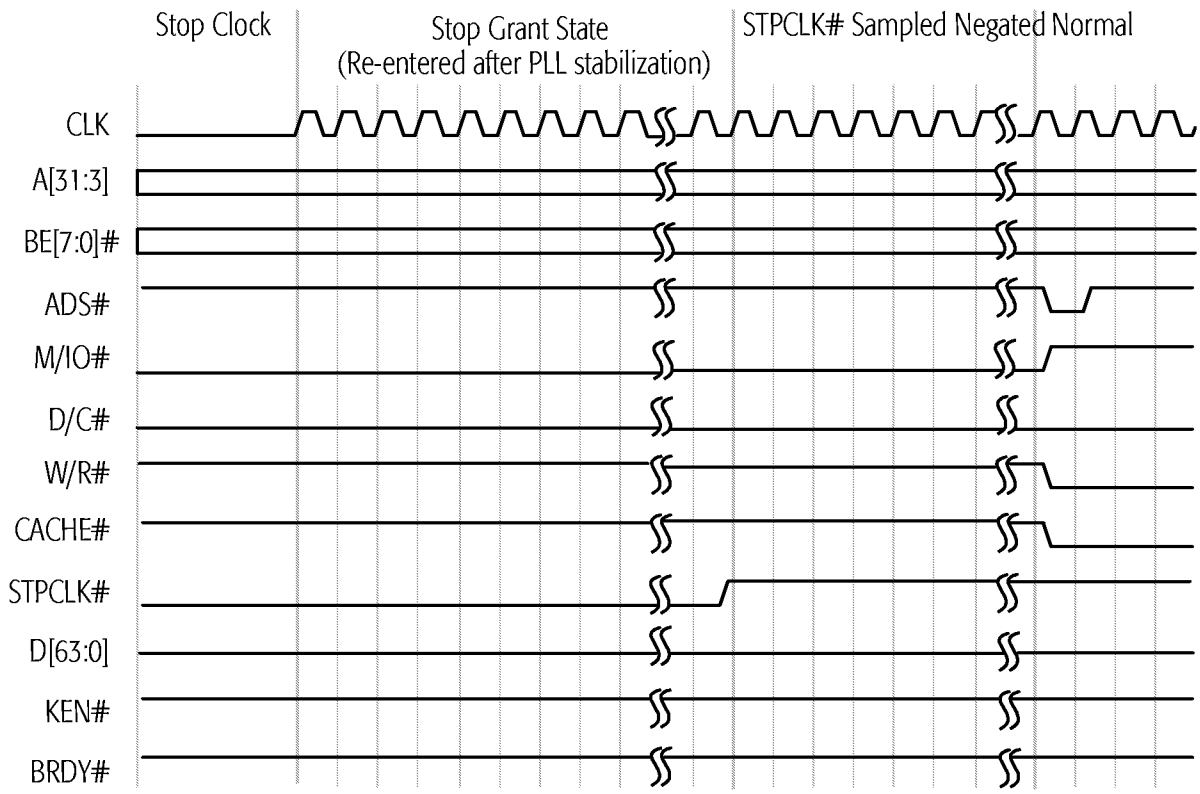

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

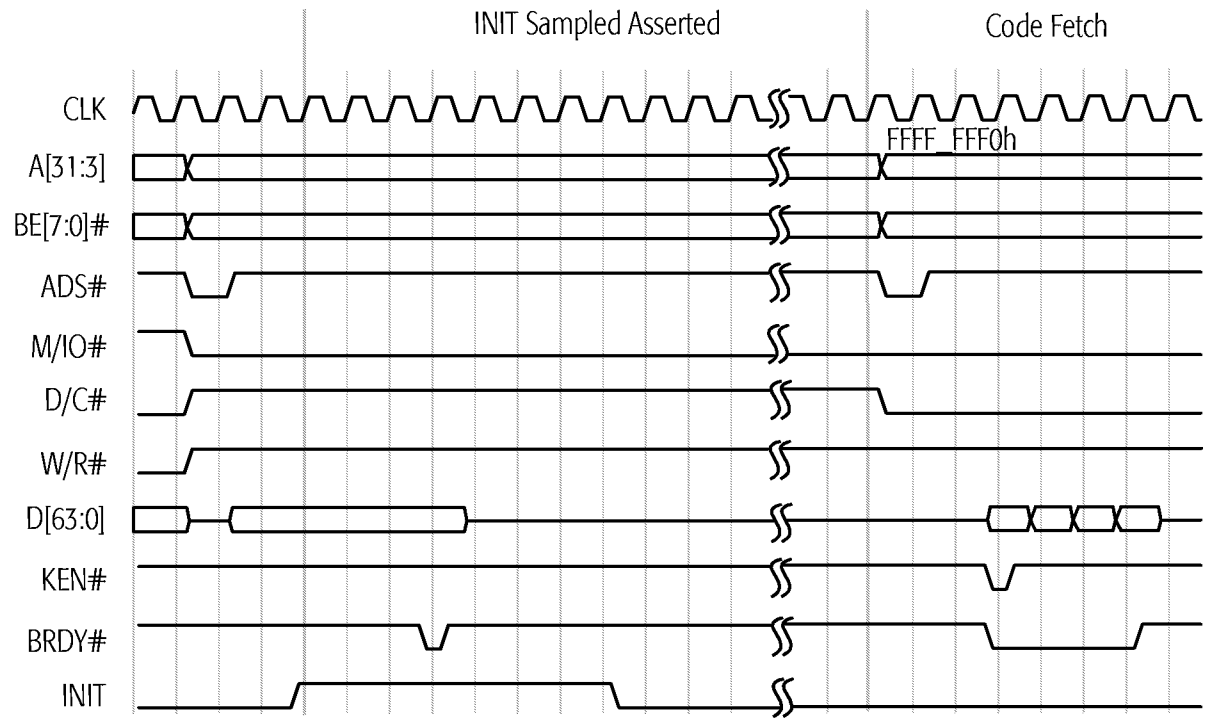

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.